1972

# A Study of Monolithic Circuit Components

Mahendra Pratap Agrawal

A STUDY OF MONOLITHIC CIRCUIT COMPONENTS

This thesis is approved as a creditable and independent investigation by a candidate for the degree, Master of Science, and is acceptable as meeting the thesis requirements for this degree. Acceptance of this thesis does not imply that the conclusions reached by the candidate are necessarily the conclusions of the major department.

Thesis Adviser Date / /

Head, Electrical Engineering Department Date / /

ACKNOWLEDGEMENT

The author wishes to express his sincere gratitude and appreciation to Dr. F. C. Fitchen who directed this thesis and provided both insight and inspiration in a number of areas.

Special thanks for the efforts are due to Dr. V. G. Ellerbruch. Dr. Ellerbruch helped to crystallize the thoughts through fruitful discussions.

This research was supported by the National Science Foundation.

Finally, to those who have been overlooked in this acknowledgement the author expresses his gratitude.

Mahendra Pratap Agrawal

TABLE OF CONTENTS

Page

# LIST OF FIGURES

Figure Number

Figure Number — Page

Figure Number

Figure Number

# LIST OF TABLES

Table
Number

# CHAPTER I

## INTRODUCTION

In an integrated circuit both active and passive circuit elements are formed by diffusions into a silicon substrate (usually p-type). Circuit elements must be isolated from each other and this is usually accomplished with diffused p-n junctions that form back to back diodes. Although adequate isolation is obtained, the structures have several inherent detrimental parasitic effects. These include substrate transistor action, parasitic capacitance at each junction, etc. The equivalent circuits of resistors, capacitors, diodes and transistors in an integrated structure, therefore, are different from those used for discrete components. The integrated resistor can illustrate most of the parasitic effects. The resistor has both a distributed capacitance and a distributed transistor effect. The n-type layer, which is used for isolation, becomes the base of a low beta p-n-p transistor.

This research is concerned with the study of some monolithic circuit components--resistors and the p-n junctions of diodes and transistors. Because of the parasitic effects, these studies are original and valuable. The thesis is arranged in three sections. The first section is devoted to the parasitic effects in diffused resistors. As already noted, the distributed capacitance effects arising due to the capacitance of p-n junctions changes the equivalent circuit of

resistors. Therefore, the high frequency performance of a diffused resistor is severely limited. The objective of the research was to find a suitable theoretical model for resistors which will predict input impedance magnitude and phase responses based on experimental observations. Some of the literature available[1,2,6] on the parasitic effects in diffused resistors discusses the impedance magnitude response. Phase studies showing the nature of variation of phase with frequency for actual resistors were not available. In this thesis phase studies are included because they provide important information helpful in determining suitable models for resistors.

The second section is concerned with the study of parasitic junction capacitances in diodes. Commonly, diodes are obtained using one p-n junction of a transistor. There are several possible diode connections when a transistor is used. This type of study is intended to give an insight into various junction capacitances and their total contribution in a diode. Since the simple models considered did not compare favorably with experimental results, a different comparison is made. These diodes were compared to the diodes connected from transistors on the chip. The nature of variation of capacitances when connected in different configurations are compared for the two types of diodes.

The study is concluded with the discussion of d-c characteristics of three p-n junctions which exist in a transistor, namely, emitter-base, base-collector and collector-substrate. The research starts with comparisons of the d-c characteristics of these junctions; it is

ended with consideration of d-c V-I characteristics of an individual p-n junction.

The inherent parasitic junction capacitance of diffused resistors may sometimes be used to an advantage. In some applications, such as the coupling resistor of a flip-flop circuit, a small speed up capacitor is usually placed in the parallel with the resistor. Since the diffused resistor has some parasitic capacitance, it may be used as the speed up capacitor. It is assumed that this research will provide useful information for persons involved in designing circuits using monolithic components.

# CHAPTER II

# DIFFUSED RESISTORS

## 2.1 Monolithic Resistors

Perhaps the most widely used method of fabrication of microcircuit resistors is by solid-state diffusion into a background region of opposite conductivity type. These resistors are far from ideal circuit elements; however, their almost universal adoption is based on the fact that no additional processes are needed for their fabrication.

Fig. 2.1 shows a resistor made from a p-type diffusion into an n-type background. Resistors of this type are made simultaneously with transistor base diffusion in a monolithic integrated circuit.

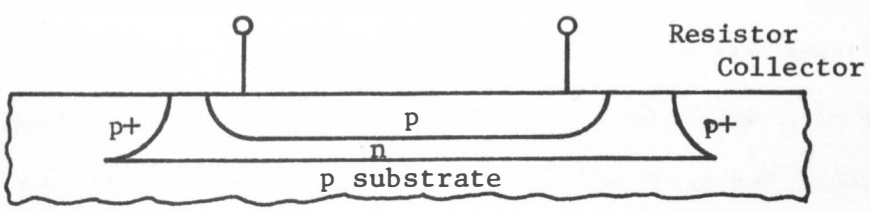



Fig. 2.1 Diffused resistor.

The resistance of this structure may be expressed as:

$$R = \rho \, L/A$$

where $\rho$, the resistivity, is the constant of proportionality which

relates the length and cross-sectional area to its resistance; $\rho$ must have the units of resistance times length. If R is in ohms, L is in cm, and A is in $cm^2$, $\rho$ will then have units of ohm-cm. If area is t by w, where w is width and t is thickness, then $\rho/t$ is defined as sheet resistance $R_s$.

Usually sheet resistance $R_s$ is limited in value since, typically, it must satisfy the design constraints of a transistor base diffusion. The resistor width is limited to a minimum value determined by photolithographic and etching techniques. Resistor length L is increased only at the expense of enlarging both the substrate area occupied by the resistor and its parasitic capacitance.

## 2.2 Parasitic Effects

Associated with a diffused resistor are a number of parasitics which must be considered in high frequency applications. Since the resistor is a p-type layer in an n-type region and the junction is reverse biased a certain amount of distributed capacitance is associated with the structure. This capacitance has the effect of limiting the frequency response of the resistor. Frequency response is the variation of the magnitude of the resistance with frequency.

For a typical semiconductor resistor made during a base diffusion, not only is there a distributed capacitance at the resistor-collector (p-n) junction, but the substrate-collector-resistor structure forms a parasitic p-n-p transistor which, in some cases, will act as a low gain transistor ($\beta \approx 0.5 - 5.0$). The equivalent circuit in lumped

form is shown in Fig. 2.2.

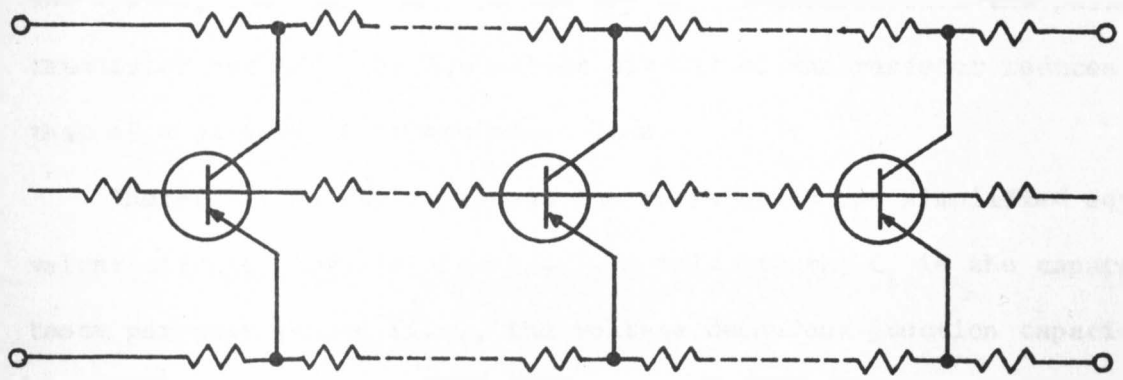


Fig. 2.2 Equivalent circuit of a diffused resistor.

A simplified version of this circuit is drawn in Fig. 2.3, from which it is seen that the resistor behaves as an active transmission line. Each capacitive element of this line is equal to the collector-base capacitance of the parasitic transistor, multiplied by its common-emitter current gain. This is highly undesirable since the characteristics of the resistor are now dependent on the gain characteristics of the transistor as well as on its collector-base capacitance.

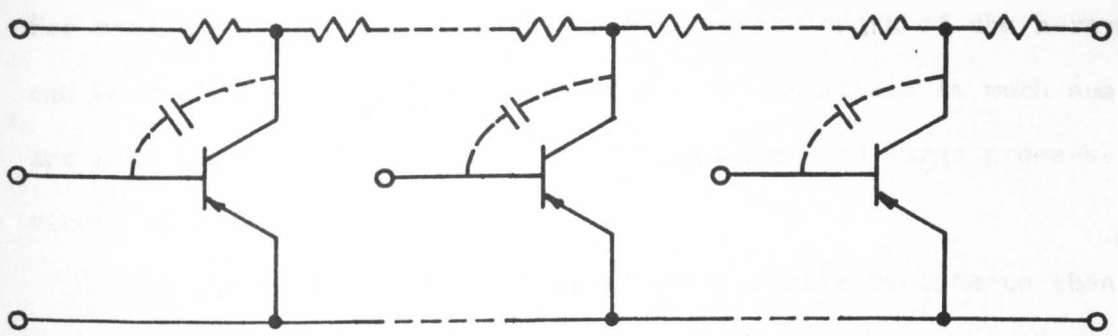


Fig. 2.3 Simplified equivalent circuit of a diffused resistor.

If the n-type epitaxial layer is tied to the most positive point in the system, the transistor is cut off at all times. With the parasitic transistor cut off, the equivalent circuit of the resistor reduces to that of a passive RC transmission line.

Therefore, we may represent the resistor by the simplified equivalent circuit shown in Fig. 2.4. In this figure, $C_\ell$ is the capacitance per unit length (i.e., the voltage dependent junction capacitance per unit area times the resistor width), and $R_\ell$ is the resistance per unit length (i.e., the resistivity divided by the cross-sectional area perpendicular to the direction of current flow) of the p-region.

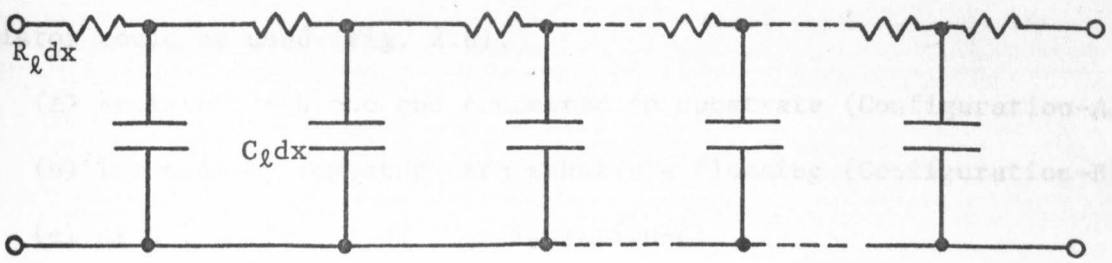



Fig. 2.4 R C line representation of a diffused resistor.

For some applications, the resistance per unit length of the n-region can be included in $R_\ell$, but in practice this resistance is much smaller than that of the resistor itself because of the large cross-sectional area of the n-layer.

If the substrate is also considered to have resistance then the RC line representation shown before is modified to that shown in Fig. 2.5. In the figure NR represents substrate resistance with the resistivity of the substrate being taken as N times that of p-type resistor

layer (factor N is less than 1).

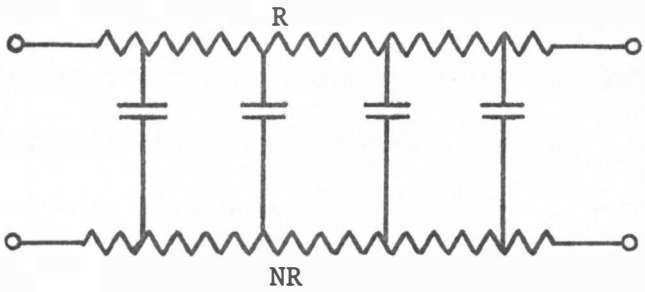



Fig. 2.5 Distributed RC network representation of a diffused resistor including substrate resistance.

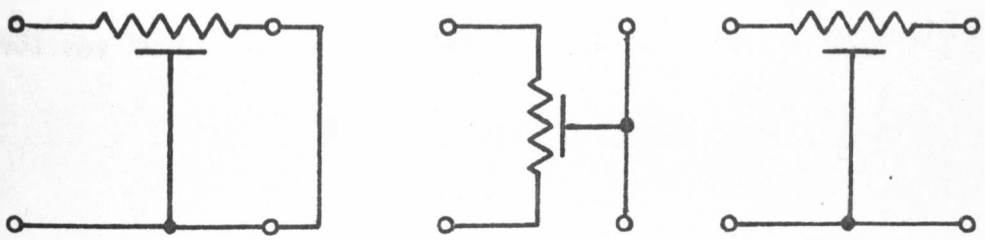
## 2.3 Three Different Configurations

In practice there are three different configurations in which a resistor could be used (Fig. 2.6).

(a) Resistor with one end connected to substrate (Configuration-A)

(b) Two ends of resistor with substrate floating (Configuration-B)

(c) As a transfer block (Configuration-C)



(a) (b) (c)

Fig. 2.6 Three configurations of a resistor.

For each of these different configurations a study of resistors was made with the aim to develop a model which closely simulates the behaviour of the actual resistor. Because in a diffused resistor the

resistance and the parasitic capacitance are not lumped but distributed over the resistor length, the need for a distributed network rather than a lumped model was realized. Each of these configurations will be considered separately in the following chapters.

Three resistors were selected for study on Quickchip SG 3801, made by Silicon General Incorporated. From the Quickchip worksheet resistors $R_{18}$, $R_{12}$, and $R_5$ (see Fig. 3.1) were selected which have values as indicated in data sheet of 600Ω, 2.5kΩ, and 10kΩ respectively with ±20% tolerance. As said before, large valued resistors need larger areas on the substrate and hence the associated parasitic capacitance is larger. Since the selected resistors range from a low value of 600Ω to a high value of 10kΩ they provide a good indication of the effect of parasitics with respect to size and value of resistor. Because of the large area needed for large valued resistors, e.g. 10kΩ, usually they are not fabricated as linear in shape. On Quickchip SG 3801 the 10 kΩ resistor appears folded as shown in Fig. 2.7.

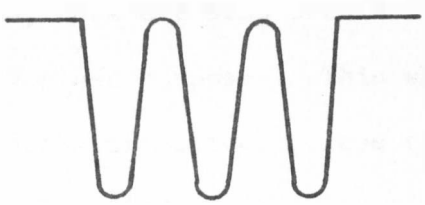


Fig. 2.7 Folded resistor.

This type of folded resistor may exhibit extra capacitance between folds so that there may be need of a more complex model.

Diffused resistors are made during the base diffusion. This diffusion process is carried out inside the collector diffused region

which provides a sort of tub for the resistor. Considering this tub for three configurations described earlier, there could be two additional possibilities of tub connection:

(a) With tub biased

(b) With tub left floating

Since the equivalent circuit of the resistor is a distributed network and there are two p-n junctions, a simple model, with tub taken into consideration, could be as in Fig. 2.8.

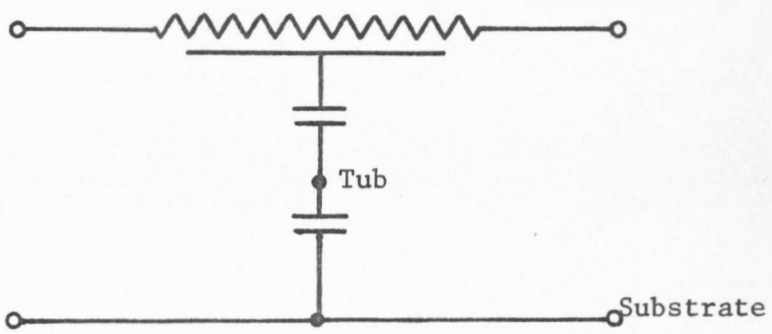



Fig. 2.8 Simplified schematic representation of diffused resistor with tub considered.

In case of tub bias, this d-c bias provides a short circuit between tub and substrate for a-c purposes. This short eliminates part of the parasitic capacitance. Effectively, less capacitance is expected than for the case of tub floating.

Since the actual connection of a diffused resistor includes the substrate, there are three terminals available--two ends of the resistor and the substrate. Figure 2.6 indicates the proper terminals used to make measurements for the three different configurations

It was decided to study effective $R_p$ and $C_p$, equivalent parallel resistance and capacitance, looking in at the input terminals. Magnitude and phase responses were obtained from these parameters. The next chapter describes the experimental setup and measurements involved.

# CHAPTER III

# RESISTOR EXPERIMENTAL CONNECTIONS

## 3.1 Experimental Setup

Frequency response measurements on diffused resistors require the measurements of magnitude and phase over a wide range of frequency. Since it is not easy to directly measure the magnitude and phase of the resistor impedance over the desired frequency range (several hundred megahertz) a different approach was adopted. Equivalent parallel resistance and parallel capacitance, $R_p$ and $C_p$, were measured using type 250-A Boonton Radio Co. RX-Meter. Later on, these $R_p$ and $C_p$ measurements were converted to the magnitude and phase form.

Fig. 3.1 shows the worksheet of Quickchip SG 3801 from which resistor elements were selected and studied. The SG 3801 quickchip is a monolithic breadboard containing over 50 separate components of various types and values. Because these components can be connected with nothing more than a wire bonding machine, it is easy to study different kinds of resistors. As shown in Fig. 3.1 different resistors were bonded to pins as follows.

| | |
|---|---|
| Resistor $R_{18}$ (600Ω) | Pins 1 and 2 |
| Resistor $R_{12}$ (2.5KΩ) | Pins 3 and 5 |
| Resistor $R_5$ (10KΩ) | Pins 8 and 9 |

APPLICATIONS DATA

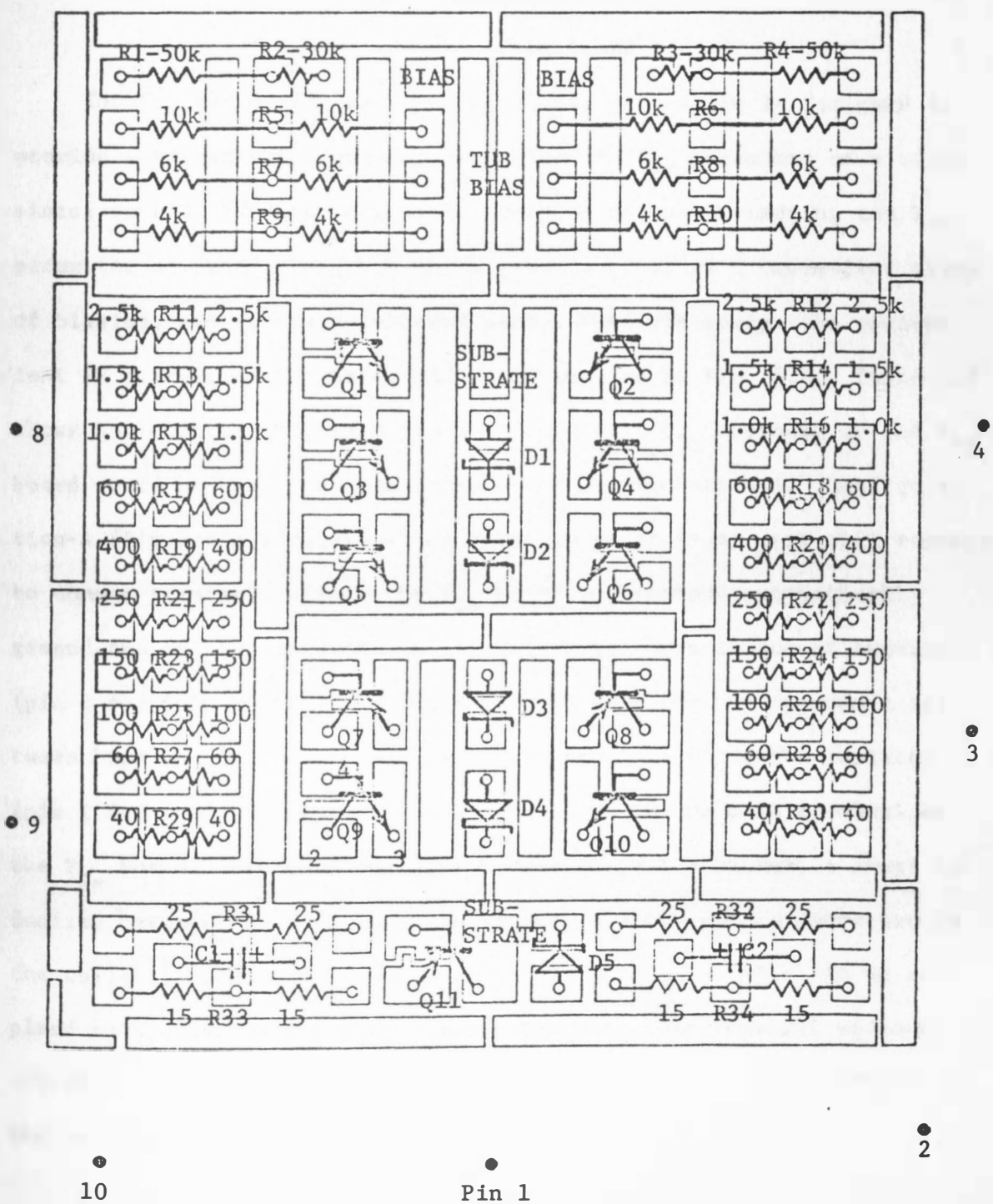
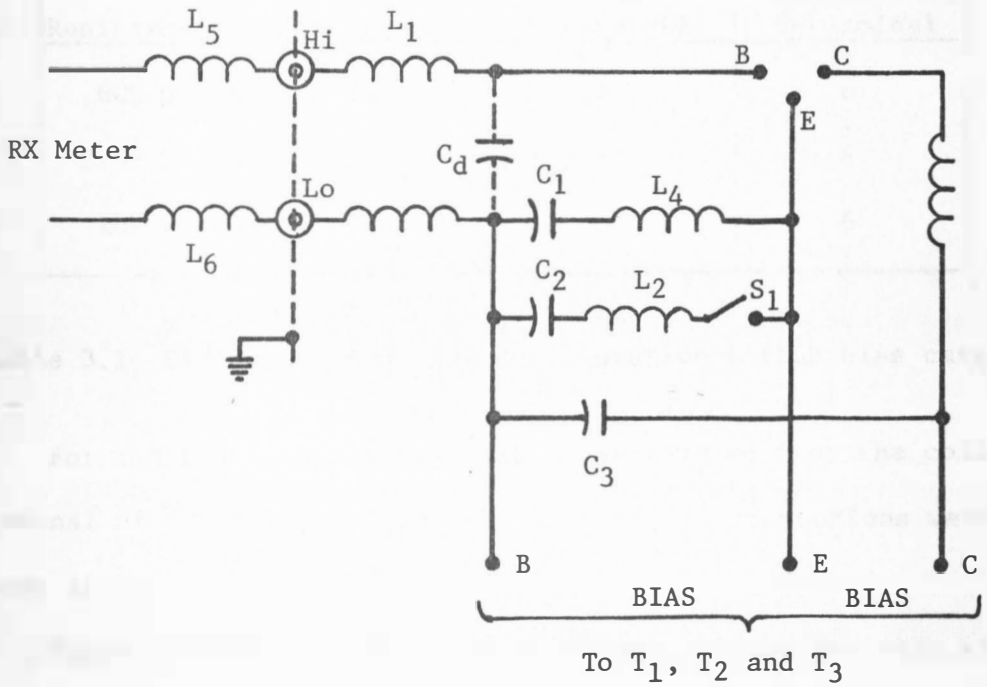



Fig. 3.1 Quickchip SG 3801 worksheet.

| | |
|---|---|
| Substrate | Pin 4 |
| Tub | Pins 6 and 7 |

The $Y_{ie}$ board, 13510A transistor test jig, which is designed to provide a convenient means for measuring the $Y_{ie}$ parameter of a transistor on 250A RX Meter was used. Here we are not measuring the $Y_{ie}$ parameter of transistor, but the $Y_{ie}$ board provides a convenient means of biasing, and it was considered useful for this study. An equivalent RF circuit of the meter and board appears in Fig. 3.2. Table 3.1 shows how emitter (E), base (B) and collector (C) terminals of the $Y_{ie}$ board could be used for measurements for configuration-A. Configuration-A (Fig.2.6(a)) requires the measurement at input port with respect to common terminal. Since the $Y_{ie}$ board connections automatically ground the emitter terminal it can be treated here as common terminal (pin 2 for 600Ω resistor). The $Y_{ie}$ board measures the impedance between base and emitter terminals, so other terminal of the resistor (pin 1 for 600Ω resistor) could be connected to the base terminal of the $Y_{ie}$ board. Since in tub biased case for a-c purposes, a short is desired between tub and common terminals, the tub can be connected to the collector terminal of the $Y_{ie}$ board. Here a d-c bias can be applied to the tub by applying bias to the collector terminal without altering a-c connections. For the tub floating case no connection to the collector terminal is required.




$C_d$ - Distributed capacity of high terminals (2.5pF nominal)

$C_1$ - 29μF - 30V capacitor

$C_2$ - 0.1μF - 50V capacitor

$C_3$ - same as $C_2$

$L_1$ - 3nh lead and terminal inductances

$L_2$ - 4nh lead and terminal inductances

$L_3$ - 8.5nh lead and terminal inductances

$L_4$ - 34nh lead and terminal inductances

$L_5$,$L_6$ - 3nh RX Meter terminal inductance

$S_1$ - RF switch

$T_{1-3}$ - Bias Terminals

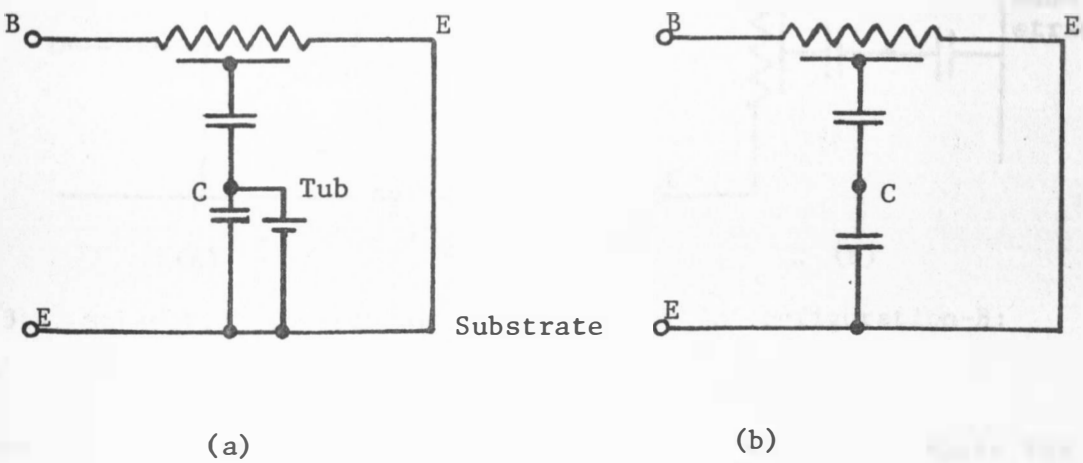
Fig. 3.2 Equivalent RF circuit for $Y_{ie}$ jig board.

| Resistance | Pin Connected to E-terminal | Pin Connected to B-terminal | Pin Connected to C-terminal |
|---|---|---|---|
| 600 Ω | 2 ,4 | 1 | 6 |
| 2.5k Ω | 3 ,4 | 5 | 6 |
| 10k Ω | 9 ,4 | 8 | 6 |

Table 3.1 Pin connections for configuration-A (tub bias case).

For the tub-floating case pin 6 was removed from the collector terminal of the $Y_{ie}$ board and the rest of the connections were as shown in Table 3.1 above.

Figure 3.3 shows the schematic circuit of the resistor with the $Y_{ie}$ board pin connections made for configuration-A (Table 3.1).




(a) (b)

Fig. 3.3 Schematic representation of a resistor in configuration-A: (a) tub biased case; (b) tub floating.

For configuration-B Table 3.2 gives the pin connections used on the $Y_{ie}$ board to make measurements.

| Resistance | Pin Connected to E-terminal | Pin Connected to B-terminal | Pin Connected to C-terminal |
|---|---|---|---|
| 600Ω | 2 | 1 | 6 |
| 2.5KΩ | 3 | 5 | 6 |
| 10KΩ | 9 | 8 | 6 |

Table 3.2 Pin connections for configuration-B (tub bias case).

Again pin-6 was removed when the tub floating case was studied. Fig. 3.4 shows the schematic circuit of resistor with proper pin connections for configuration-B.

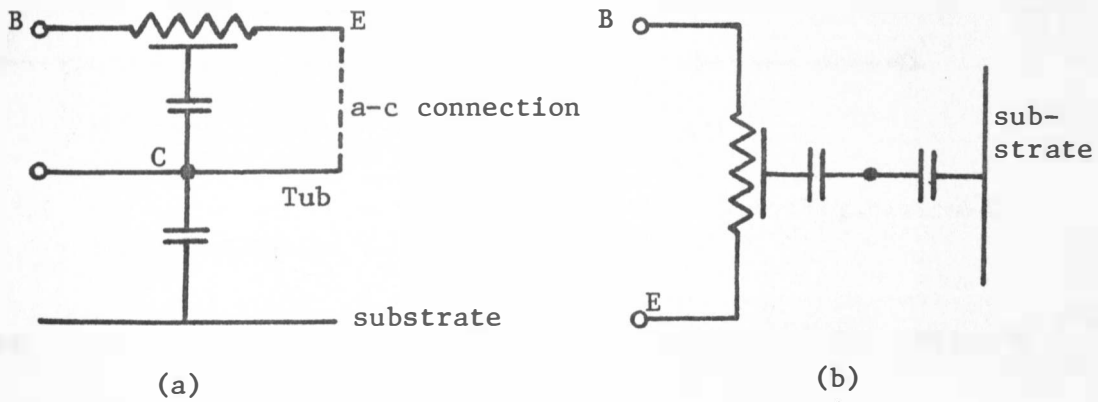



Fig. 3.4 Schematic representation of resistor in configuration-B: (a) tub biased; (b) tub floating.

For configuration-C pin connections are given in Table 3.3. Again for the tub floating case pin 6 was removed from the collector terminal of the $Y_{ie}$ board. Fig. 3.5 gives the schematic circuit with proper pin connections for this case. The following chapter presents the data collected using the setups described here for three different resistors

| Resistance | Pin Connection to E | Pin Connection to B | Pin Connection to C |
|---|---|---|---|
| 600Ω | 4 | 1 | 6 |
| 2.5KΩ | 4 | 5 | 6 |
| 10KΩ | 4 | 8 | 6 |

Table 3.3 Pin connections for configuration-C (tub bias case).

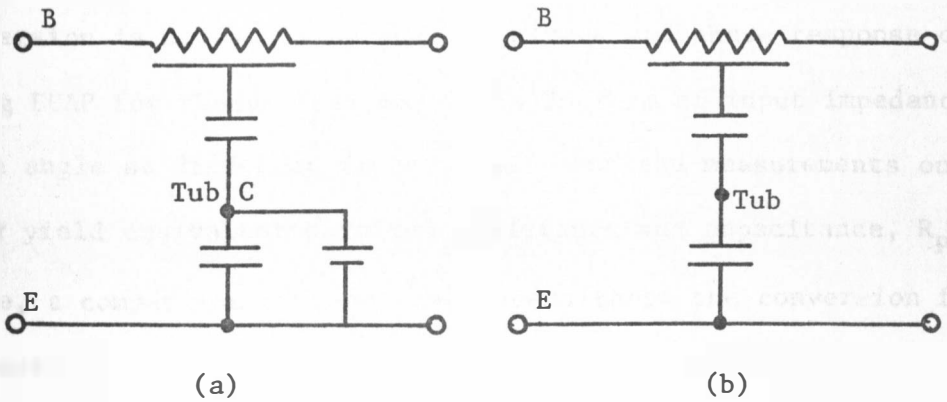



Fig. 3.5 Schematic representation of resistor in configuration-C: (a) tub biased; (b) tub floating.

and for three different configurations; development of the resistor model follows from the data.

# CHAPTER IV

## MEASUREMENTS AND DEVELOPMENT OF RESISTOR MODEL

Equivalent parallel resistance $R_p$ and parallel capacitance $C_p$ measurements were converted into magnitude and phase responses. This conversion is necessary because magnitude and phase response obtained using ECAP for theoretical models is in form of input impedance and phase angle at different frequencies. But the measurements on the RX meter yield equivalent parallel resistance and capacitance, $R_p$ and $C_p$. Hence, a comparison of these two necessitates the conversion from one to another. A description of this conversion follows.

To obtain the magnitude of Z and the corresponding phase angle, $R_p$ and $C_p$ were measured on the RX Meter and then converted to magnitude of Z and phase. $R_p$ and $C_p$ are the effective parallel resistance and capacitance that appear at the input terminals. To obtain the magnitude and phase of Z, $R_p$ and $C_p$, measurements were transformed by the following relationship.

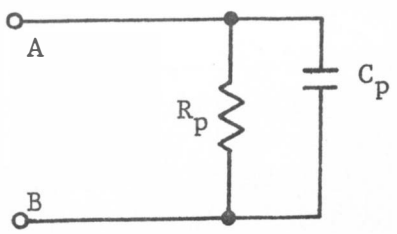



Fig. 4.1 Parallel equivalent $R_p$ and $C_p$ circuit.

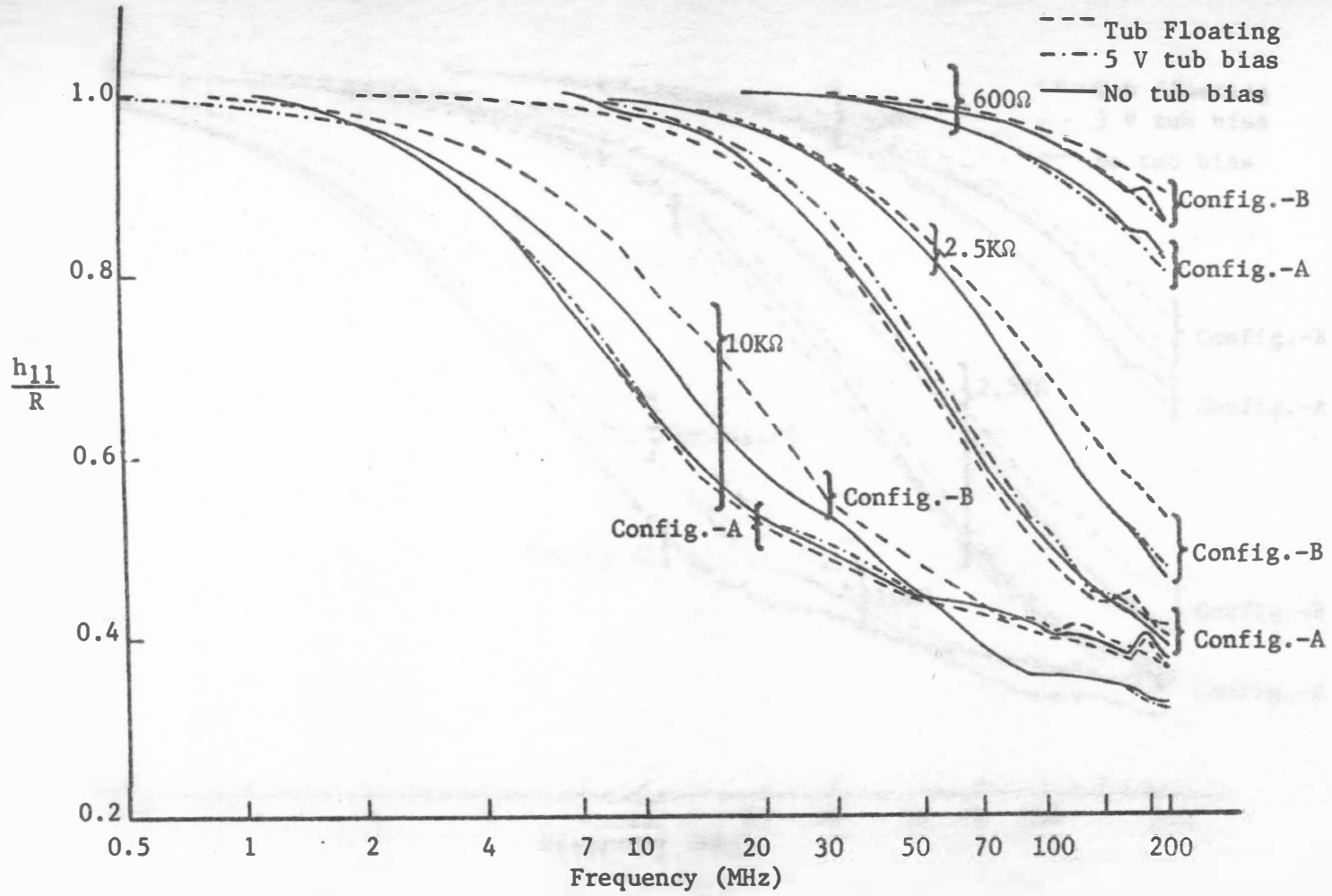



Fig. 4.2 Impedance ratio vs. frequency responses for three different resistors.

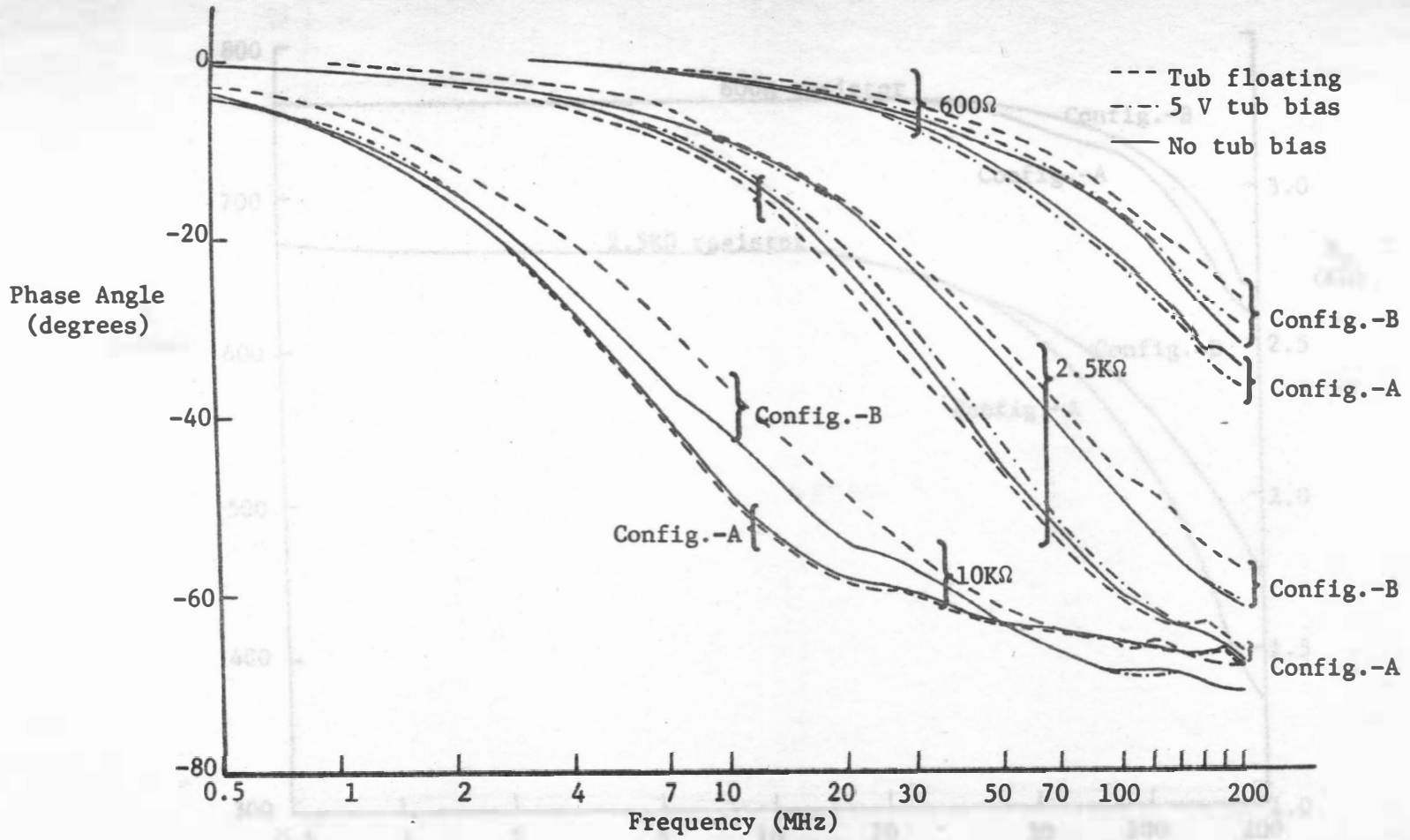



Fig. 4.3 Phase angle vs. frequency responses for three different resistors.

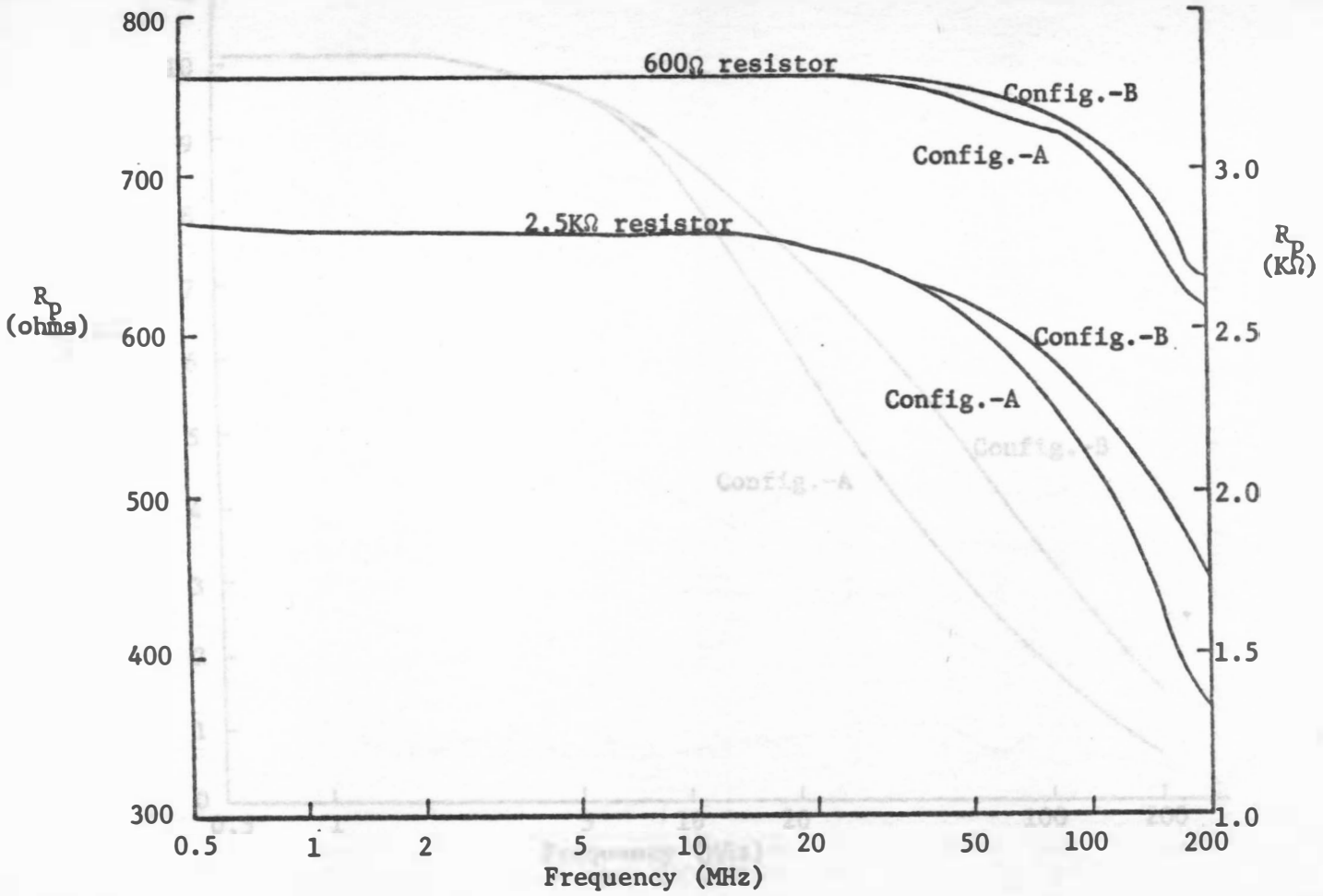



Fig. 4.4 (a) Equivalent parallel resistance vs. frequency for 600Ω and 2.5KΩ resistors.

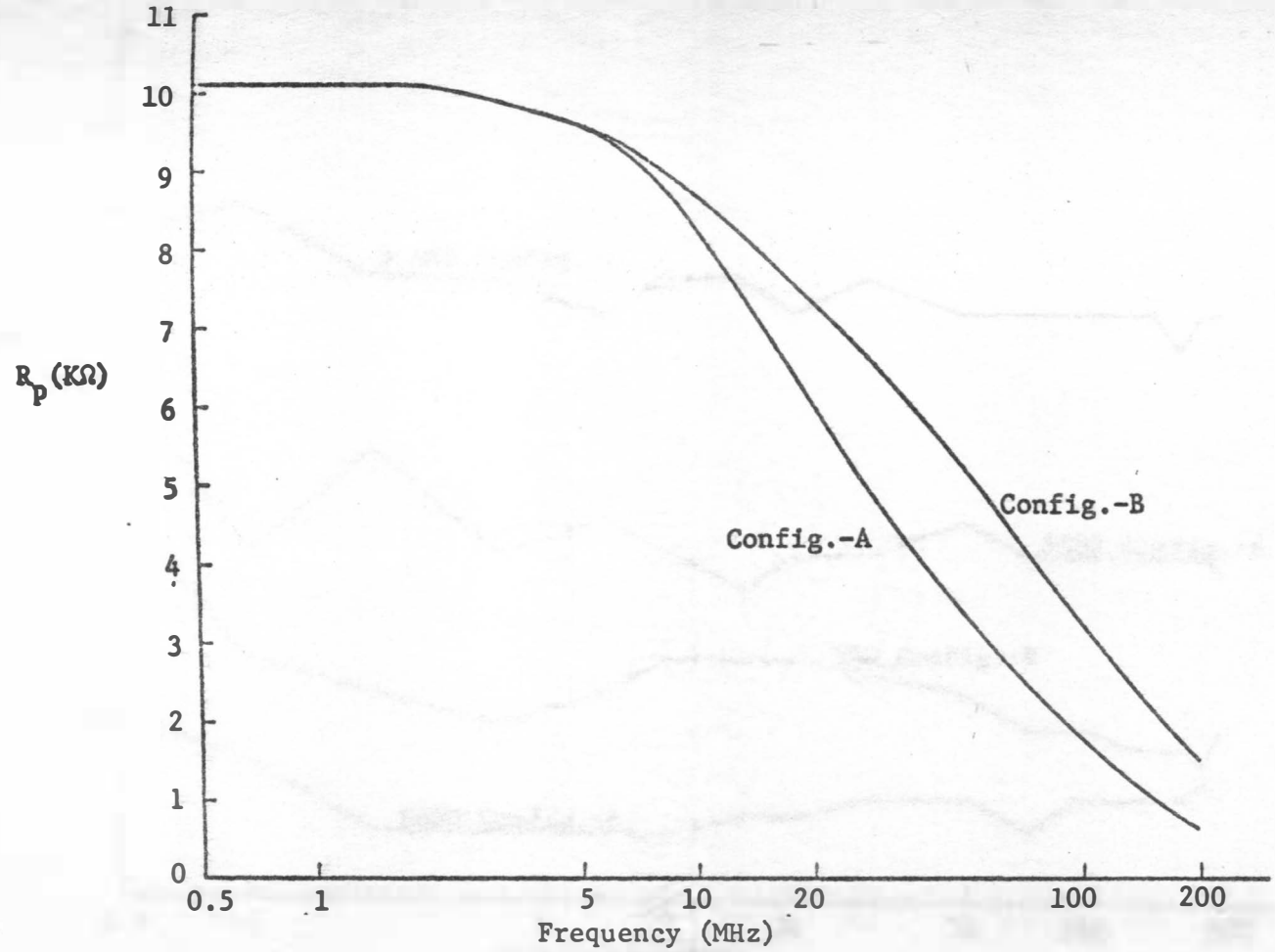



Fig. 4.4(b) Equivalent parallel resistance vs. frequency for 10KΩ resistor.

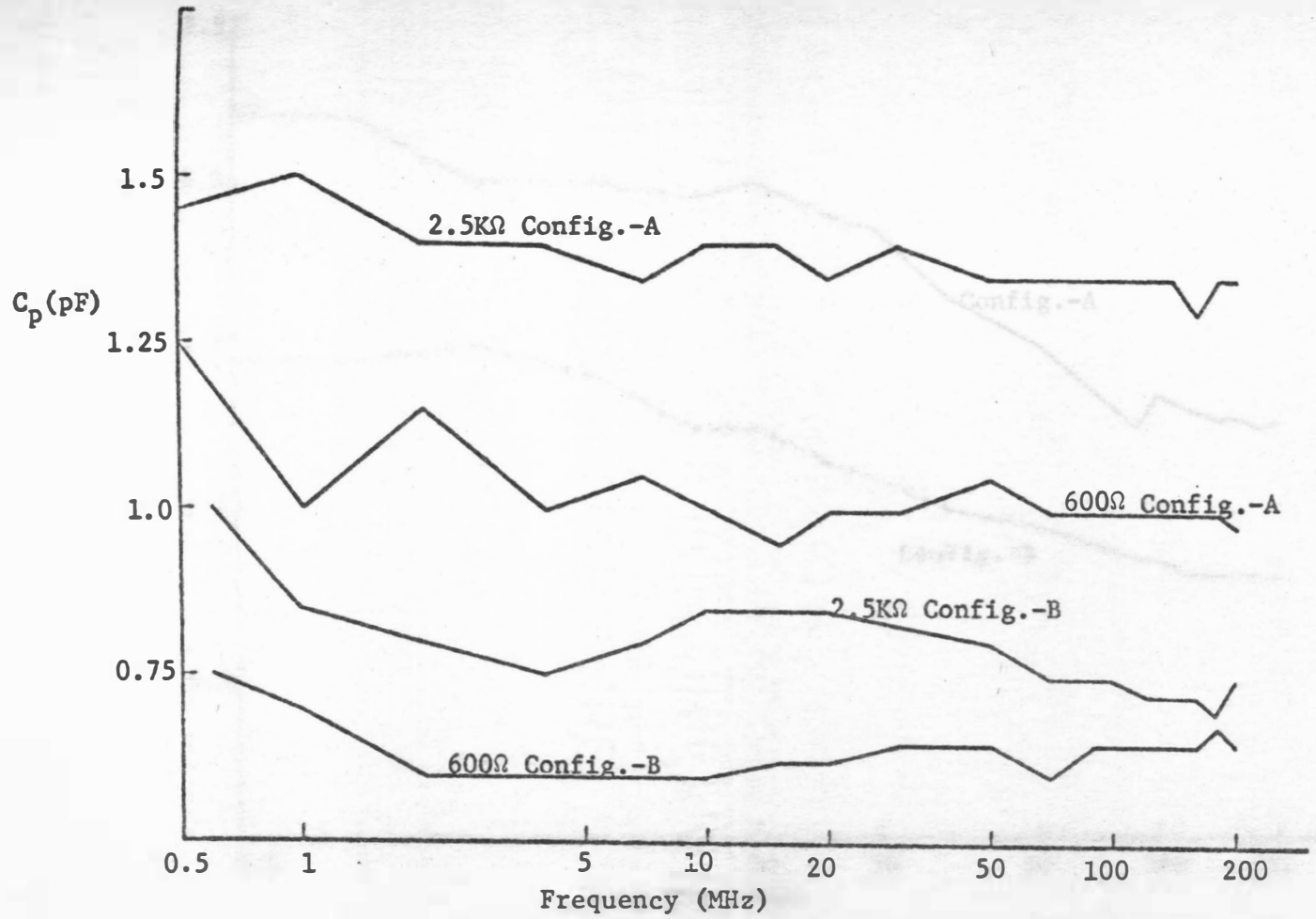



Fig. 4.5(a) Equivalent parallel capacitance vs. frequency for 600Ω and 2.5KΩ resistor.

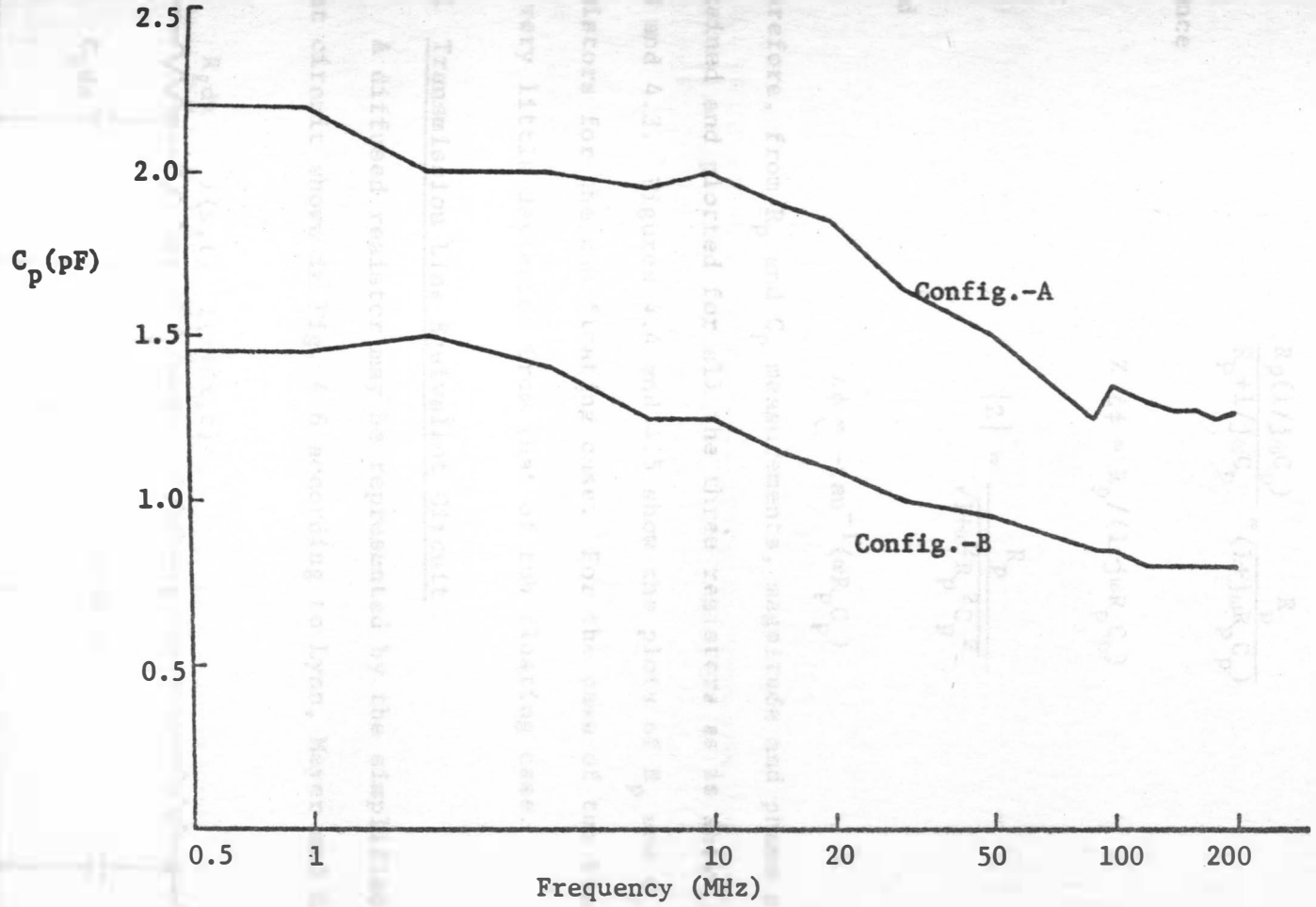



Fig. 4.5 (b) Equivalent parallel capacitance vs. frequency for 10KΩ resistor.

Impedance looking in at terminals A and B is:

$$\frac{R_p(1/j\omega C_p)}{R_p+1/j\omega C_p} = \frac{R_p}{(1+j\omega R_p C_p)}$$

Hence

$$Z\ \angle\phi = R_p/(1+j\omega R_p C_p)$$

or

$$|Z| = \frac{R_p}{\sqrt{1+\omega^2 R_p^2 C_p^2}} \tag{4.1}$$

and

$$\angle\phi = -\tan^{-1}(\omega R_p C_p) \tag{4.2}$$

Therefore, from $R_p$ and $C_p$ measurements, magnitude and phase of Z were obtained and plotted for all the three resistors as is shown in Figs. 4.2 and 4.3. Figures 4.4 and 4.5 show the plots of $R_p$ and $C_p$ for three resistors for the tub floating case. For the case of tub biased there is very little deviation from that of tub floating case.

## 4.1 Transmission Line Equivalent Circuit

A diffused resistor may be represented by the simplified equivalent circuit shown in Fig. 4.6 according to Lynn, Meyer and Hamilton.[5]

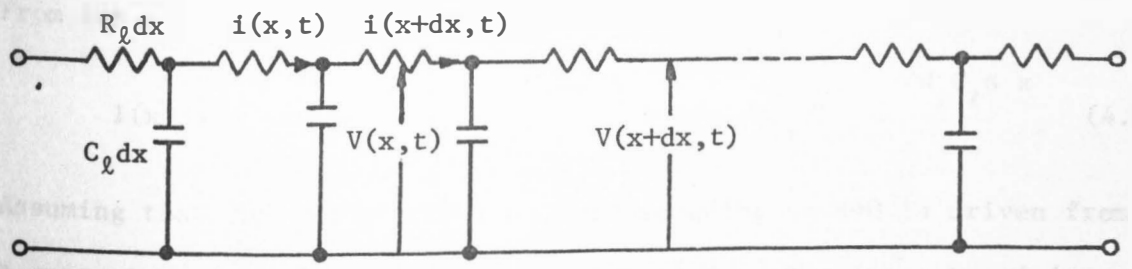



Fig. 4.6 Simplified equivalent circuit of a diffused resistor.

In this figure $C_\ell$ is the capacitance per unit length and $R_\ell$ is the resistance per unit length. The differential equations for the circuit of Fig. 4.6 are

$$\frac{\partial V}{\partial x} = -R_\ell i \tag{4.3}$$

$$\frac{\partial i}{\partial x} = -\bar{C}_\ell \frac{\partial V}{\partial t} \tag{4.4}$$

or

$$\frac{\partial^2 V(x,t)}{\partial x^2} = -R_\ell \frac{\partial i}{\partial x} = R_\ell \bar{C}_\ell \frac{\partial V(x,t)}{\partial t} \tag{4.5}$$

$$\frac{\partial^2 i(x,t)}{\partial x^2} = +R_\ell \bar{C}_\ell \frac{\partial i(x,t)}{\partial t} \tag{4.6}$$

Eqns. (4.5) and (4.6) are the standard relationships incurred in the analysis of RC transmission lines.

Using the Laplace transform, and assuming zero initial conditions, we obtain from Eqn. (4.5)

$$\frac{\partial^2 V(x,s)}{\partial x^2} = R_\ell \bar{C}_\ell s V(x,s) \tag{4.7}$$

The solution of (4.7) has the form

$$V(x,s) = A(s)\, e^{\sqrt{R_\ell \bar{C}_\ell s}\, x} + B(s)\, e^{-\sqrt{R_\ell \bar{C}_\ell s}\, x} \tag{4.8}$$

From Eqn. (4.6) we get

$$I(x,s) = -A(s)\sqrt{s\bar{C}_\ell / R_\ell}\, e^{\sqrt{s\bar{C}_\ell R_\ell}\, x} + B(s)\sqrt{s\bar{C}_\ell / R_\ell}\, e^{-\sqrt{R_\ell \bar{C}_\ell s}\, x} \tag{4.9}$$

Assuming that the end of the line corresponding to x=0 is driven from a current source I(s) and that the other end of the line at $x=\ell$ is terminated in an impedance $Z_t(s)$, we obtain the following boundary

conditions:

$$x=0 \qquad I(o,s) = I(s)$$

$$x=\ell \qquad V(\ell,x) = Z_t(s)I(\ell,s)$$

from which the coefficients A and B can be determined.

Solving for A and B and putting these back into Eqns. (4.8) and (4.9) we obtain the general expression for the voltage and current along the line:

$$V(x,s) = \sqrt{R_\ell/s\bar{C}_\ell}\,\frac{\left\{\left[1+Z_t(s)\sqrt{s\bar{C}_\ell/R_\ell}\right]e^{-\sqrt{R_\ell\bar{C}_\ell s}(x-\ell)} - \left[1-Z_t(s)\sqrt{s\bar{C}_\ell/R_\ell}\right]e^{\sqrt{R_\ell\bar{C}_\ell s}(x-\ell)}\right\}I(s)}{e^{\sqrt{R_\ell\bar{C}_\ell s}\,\ell} + e^{-\ell\sqrt{R_\ell\bar{C}_\ell s}} + Z_t(s)\sqrt{s\bar{C}_\ell/R_\ell}\left[e^{\ell\sqrt{R_\ell\bar{C}_\ell s}} - e^{-\ell\sqrt{R_\ell\bar{C}_\ell s}}\right]} \tag{4.10}$$

$$I(x,s) = \frac{\left\{\left[1+Z_t(s)\sqrt{s\bar{C}\,\ell/R_\ell}\right]e^{-\sqrt{R_\ell\bar{C}_\ell}(x-\ell)} + \left[1-Z_t(s)\sqrt{s\bar{C}_\ell/R_\ell}\right]e^{\sqrt{R_\ell\bar{C}_\ell s}(x-\ell)}\right\}I(s)}{e^{\sqrt{R_\ell\bar{C}_\ell s}\,\ell} + e^{-\sqrt{R_\ell\bar{C}_\ell s}\,\ell} + Z_t(s)\sqrt{s\bar{C}_\ell/R_\ell}\left[e^{\ell\sqrt{R_\ell\bar{C}_\ell s}} - e^{-\ell\sqrt{R_\ell\bar{C}_\ell s}}\right]} \tag{4.11}$$

At the end of the line that is being driven by a current generator, the voltage and current are related by

$$V(o,s) = \sqrt{R_\ell/s\bar{C}_\ell}\,\frac{\left[1+Z_t(s)\sqrt{s\bar{C}_\ell/R_\ell}\right]e^{\ell\sqrt{R_\ell\bar{C}_\ell s}} - \left[1-Z_t(s)\sqrt{s\bar{C}_\ell/R_\ell}\right]e^{-\ell\sqrt{R_\ell\bar{C}_\ell s}}}{e^{\ell\sqrt{R_\ell\bar{C}_\ell s}} + e^{-\ell\sqrt{R_\ell\bar{C}_\ell s}} + Z_t(s)\sqrt{s\bar{C}_\ell/R_\ell}\left[e^{\ell\sqrt{R_\ell\bar{C}_\ell s}} - e^{-\ell\sqrt{R_\ell\bar{C}_\ell s}}\right]}\,I(s) \tag{4.12}$$

If the output end is shorted, i.e. $Z_t(s)=0$, the input impedance of the RC line becomes

$$Z_{in}(s) = \frac{V(o,s)}{I(s)} = \frac{R_\ell \cdot \ell}{\sqrt{R_\ell C_\ell \ell^2 s}\ \mathrm{Coth}\sqrt{R_\ell \ell C_\ell \ell s}} \tag{4.13}$$

Let

$R_\ell \cdot \ell = R$ Total resistance

$\bar{C}_\ell \cdot \ell = \bar{C}$ Total average capacitance.

Then

$$Z_{in}(s) \text{ or } h_{11} = \frac{R}{\sqrt{R\bar{C}s}\ \mathrm{Coth}\ \sqrt{R\bar{C}s}}$$

or

$$\frac{h_{11}}{R} = \frac{\tanh\sqrt{R\bar{C}s}}{\sqrt{R\bar{C}s}} \tag{4.14}$$

If the output port is open circuited, i.e. $Z_t(s)=\infty$, then

$$\frac{V(o,s)}{I(o,s)} = \sqrt{R_\ell/s\bar{C}_\ell}\ \sqrt{s\bar{C}_\ell/R_\ell}\ \frac{e^{\sqrt{R\bar{C}s}} + e^{-\sqrt{R\bar{C}s}}}{\sqrt{s\bar{C}_\ell/R_\ell}\left(e^{\sqrt{R\bar{C}s}} - e^{-\sqrt{R\bar{C}s}}\right)}$$

Amplitude and phase response predicted by Eqn. (4.14) are shown in Fig. 4.7. Note that high frequency attenuation rolls off at 10dB/decade and the phase angle approaches $45^o$ in the limit. Both these characteristics are half of those for a lumped parallel RC network. Note also that amplitude is down 3 dB at $2\omega RC$ instead of at $\omega RC$ as for the lumped circuit.

Now we compare the magnitude and phase responses (Fig. 4.7(a) and 4.7(b)) of theoretical transmission line model with the experimentally observed magnitude and phase responses (for three different values of resistors). It is observed that in Fig. 4.7(b) phase oscillates

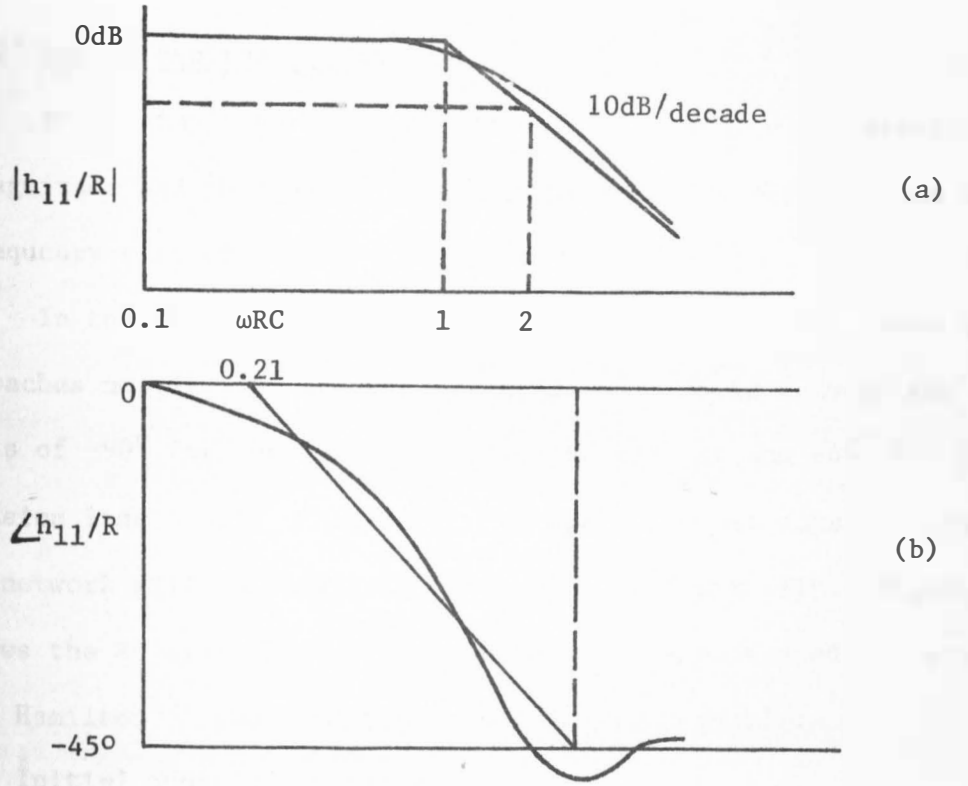



Fig. 4.7 (a) Magnitude response (b) Phase response for a distributed shorted RC network.

around $-45^{o}$ at high frequencies, while the measured phase angle given in Figs. 4.13 and 4.15 seems to monotonically increase and tends to settle down in vicinity of $-65^{o}$ (for 2.5KΩ and 10KΩ resistors). The general nature of variation in impedance $|Z|$ seems to be the same for both the theoretical transmission line and the diffused resistors, but little can be concluded at this point. It could be observed that the Fig. 4.6 model would not be applicable for our diffused resistors on the chip.

## 4.2 Lumped Equivalent Model

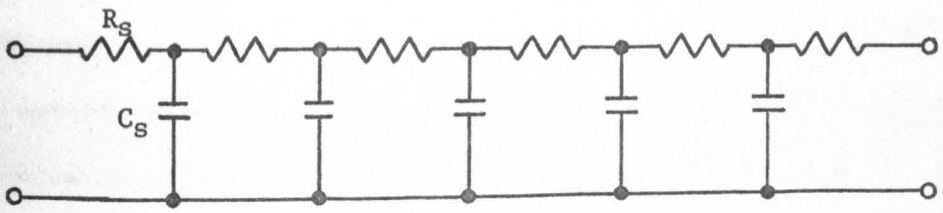
For a simple parallel RC circuit in impedance characteristics (magnitude and phase), the phase angle will approach-90° and high frequency roll off will be 6 dB/octave.

In the experimentally observed phase response the phase angle approaches nearly -70° at high frequencies which is between the two limits of -90° for the lumped parallel RC circuit and -45° for the transmission line model. Therefore, perhaps a few sections of distributed RC network will constitute a good model to start with. Figure 4.8 shows the RC distributed ladder network. As suggested by Lynn, Meyer and Hamilton[5] two variations to this are possible:

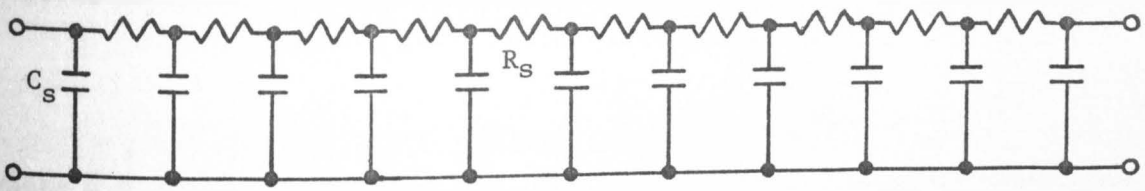
(a) Initial shunt capacitance.

(b) Initial series resistance.

These are shown in Figs. 4.8 (a) and (b) respectively.




(a)




(b)

Fig. 4.8 RC distributed network (a) 5 section initial series resistance (b) 10 section initial shunt capacitance.

The initial shunt capacitance network (Fig. 4.8(b)) was preferred in the beginning over the initial series resistance network because the former provides larger phase angle responses. ECAP was used to find the impedance characteristics (magnitude and phase) of these networks theoretically.

To determine the values of $R_s$ and $C_s$ to be used in the distributed network suggested by Lynn, Meyer and Hamilton[5], the equations used for a 5 section network are:

$$R_s = R_T/5 \quad \text{and} \quad C_s = C_T/6$$

where $R_T$ is total resistance and $C_T$ total capacitance in the circuit. Hence the value of R could be chosen by dividing total resistance by factor of 5.

Since the measurements of $C_p$ performed thus far do not provide us with a measure of $C_T$, determination of sectional capacitance $C_s$ is not straightforward. To get some idea of the value of $C_s$ to be used, it was assumed that the cut off relationship given by Ghandhi[3] holds. This cutoff frequency relationship is valid only for a theoretical transmission line which, as we concluded earlier, is not an exact model for our diffused resistors. At this point, we shall assume that that expression holds for our diffused resistors,

$$\omega_o = \frac{2}{\bar{C}R} \tag{4.15}$$

where $\bar{C}$ = effective average capacitance and R = total resistance. Eqn. (4.15) holds for the case of substrate shorted to one end of the resistor only. Table 4.1 (a) lists the 0.707 points as obtained from the

experimentally observed Z magnitude responses (Fig. 4.2).

| Resistance | Frequency corresponding to 0.707 points Configuration-A (tub floating) | Frequency corresponding to 0.707 points Configuration-B (tub floating) |
|---|---|---|
| 600Ω | 5.2 MHz | 9.6 MHz |
| 2.5KΩ | 35 MHz | 60 MHz |
| 10KΩ | ∿165 MHz | >200 MHz |

Table 4.1(a) 0.707 points for experimentally observed frequency responses.

Table 4.1(b) lists the $\bar{C}$ calculated from the Eqn. (4.15) using values in Table 4.1(a). Experimentally observed values of diffused resistors (at 0.5 MHz) were used for R in Eqn. (4.15), not the nominal values indicated for these resistors on Quick chip data sheet. These values are listed in Table 4.1(b) also.

| R (on Chip) | $R_p$ (0.5MHz) | $\bar{C}$ (Configuration-A) | $\frac{\bar{C}}{11}$ | $C_s$ (Configuration-A) | | |
|---|---|---|---|---|---|---|
| 600Ω | 760Ω | 2.62 pF | 0.23pF | 0.05pF | 0.1 pF | 0.2 pF |
| 2.5KΩ | 2.85KΩ | 3.02 pF | 0.28pF | 0.22pF | 0.27pF | 0.33pF |
| 10KΩ | 11.1KΩ | 4.2 pF | 0.38pF | 0.38pF | 0.44pF | 0.48pF |

Table 4.1(b) Values of $\bar{C}$ and $C_s$ for resistors in configuration-A.

Table 4.1(b), under the column heading $C_s$ (Configuration-A) lists the three different values of capacitors that were tried as $C_s$ in the 5 section initial shunt capacitance model. Table 4.1(c) gives the three different values of $C_s$ which were tried for configuration-B.

| R | $C_s$(Configuration-B) in pF | | |
|---|---|---|---|
| 600Ω | 0.05 | 0.08 | 0.14 |
| 2.5KΩ | 0.17 | 0.22 | 0.27 |
| 10KΩ | 0.27 | 0.33 | 0.38 |

Table 4.1(c) $C_s$ values for resistors in configuration-B.

Theoretical response obtained for configurations-A and -B for the given values of capacitance were compared to the observed responses and it was found that deviation between the two is quite significant for all three resistors.

It was observed that increasing the capacitance value lowers the theoretical frequency responses. Since experimentally observed responses are lower than the present theoretical responses new increased $C_s$ values were selected. Table 4.2 lists these new $C_s$ values tried.

| R | $C_s$(Configuration-A) | $C_s$(Configuration-B) |
|---|---|---|
| 600Ω | 0.25 pF | 0.60 pF |
| 2.5KΩ | 0.40 pF | 0.45 pF |
| 10KΩ | 0.70 pF | 1.0 pF |

Table 4.2 New set of $C_s$ values for resistors.

Impedance characteristics (magnitude and phase) of 5 section initial shunt capacitance network obtained for the values of sectional capacitance $C_s$ listed in Table 4.2 also does not compare favorably with observed response for diffused resistors.

At this point it was decided to observe the effect of increasing the number of sections on the magnitude and phase responses, and to observe the effect of initial series resistance or shunt capacitance (see Fig. 4.8).

## 4.3 Effect of the Number of Segments

Four different cases were considered to explore two effects: (a) how does increasing the number of segments affect the impedance characteristics; (b) how does the initial series resistance network or initial shunt capacitance network affect the response. Again ECAP was used to find the theoretical impedance characteristic for all these networks. The four cases are:

(a) Connection of configuration-A, initial series resistance.

(b) Connection of configuration-A, initial shunt capacitance.

(c) Connection of configuration-B, initial series resistance.

(d) Connection of configuration-B, initial shunt capacitance.

The 5 segment networks for each of the previously described cases are shown in Fig. 4.9.

The values of capacitances used are listed in Table 4.3(a) for 10 segments. For 5 and 18 segments values of C were selected so that the total capacitance is the same as for 10 segments, i.e. $10C_s(10) = 18C_s(18) = 5C_s(5)$, etc. $C_s(10)$ indicates the value of $C_s$ for 10 segments. Tables 4.3(b) and 4.3(c) give values of $C_s$ for configurations-A and -B for 5 and 18 segments respectively. Figs. 4.10 through 4.15 show the magnitude and phase responses obtained for previously described

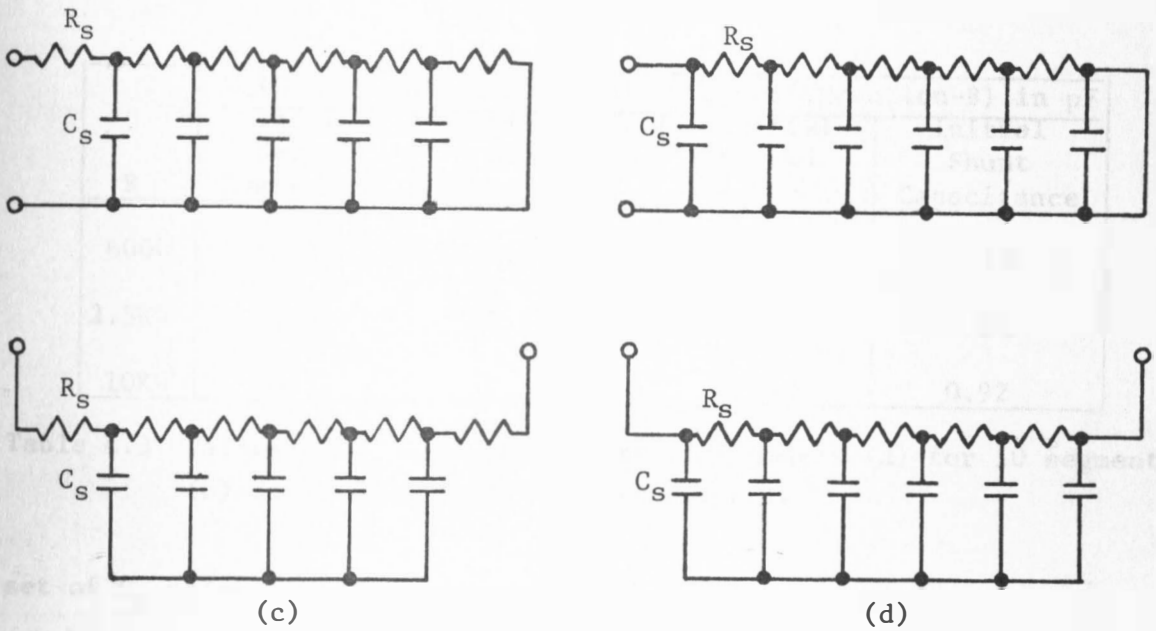



Fig. 4.9 Four different RC ladder networks for configurations-A and B.

| R | $C_S$(Configuration-A) in pF | | $C_S$(Configuration-B) in pF | |
|---|---|---|---|---|
| | Initial Series Resistance | Initial Shunt Capacitance | Initial Series Resistance | Initial Shunt Capacitance |
| 600Ω | 0.55 | 0.5 | 0.88 | 0.8 |
| 2.5KΩ | 0.55 | 0.5 | 0.88 | 0.8 |
| 10KΩ | 0.99 | 0.9 | 1.76 | 1.6 |

(a)

| R | $C_S$(Configuration-A) in pF | | $C_S$(Configuration-B) in pF | |
|---|---|---|---|---|
| | Initial Series Resistance | Initial Shunt Capacitance | Initial Series Resistance | Initial Shunt Capacitance |
| 600Ω | 1.1 | 0.92 | 1.76 | 1.47 |
| 2.5KΩ | 1.1 | 0.92 | 1.76 | 1.47 |
| 10KΩ | 1.98 | 1.65 | 3.52 | 2.93 |

(b)

| R | $C_s$(Configuration-A) in pF | | $C_s$(Configuration-B) in pF | |
|---|---|---|---|---|
| | Initial Series Resistance | Initial Shunt Capacitance | Initial Series Resistance | Initial Shunt Capacitance |
| 600Ω | 0.30 | 0.29 | 0.49 | 0.45 |
| 2.5KΩ | 0.30 | 0.29 | 0.49 | 0.45 |
| 10KΩ | 0.55 | 0.52 | 0.98 | 0.92 |

(c)

Table 4.3 Values of $C_s$ used for theoretical models (a) for 10 segment (b) for 5 segment (c) for 18 segments.

set of $C_s$ values for four cases for all three resistors.

Figures do not show all the data because some of data sets were too close to be separated from others. The following sets were too close and hence not plotted.

For 600Ω Resistor

Configuration B, Initial series resistance, 18 segments
Configuration B, Initial series resistance, 10 segments
Configuration B, Initial series resistance, 5 segments
Configuration A, Initial series resistance, 5 segments
Configuration A, Initial series resistance, 10 segments
Configuration A, Initial shunt capacitance, 18 segments

Configuration A, Initial series resistance, 5 segments
Configuration A, Initial shunt capacitance, 10 segments

Configuration B, Initial series resistance, 5 segments
Configuration B, Initial shunt capacitance, 18 segments

For 2.5KΩ Resistor

Configuration B, Initial series resistance, 5 segments
Configuration B, Initial series resistance, 10 segments
Configuration B, Initial series resistance, 18 segments

Configuration A, Initial series resistance, 5 segments
Configuration A, Initial series resistance, 10 segments
Configuration A, Initial series resistance, 18 segments

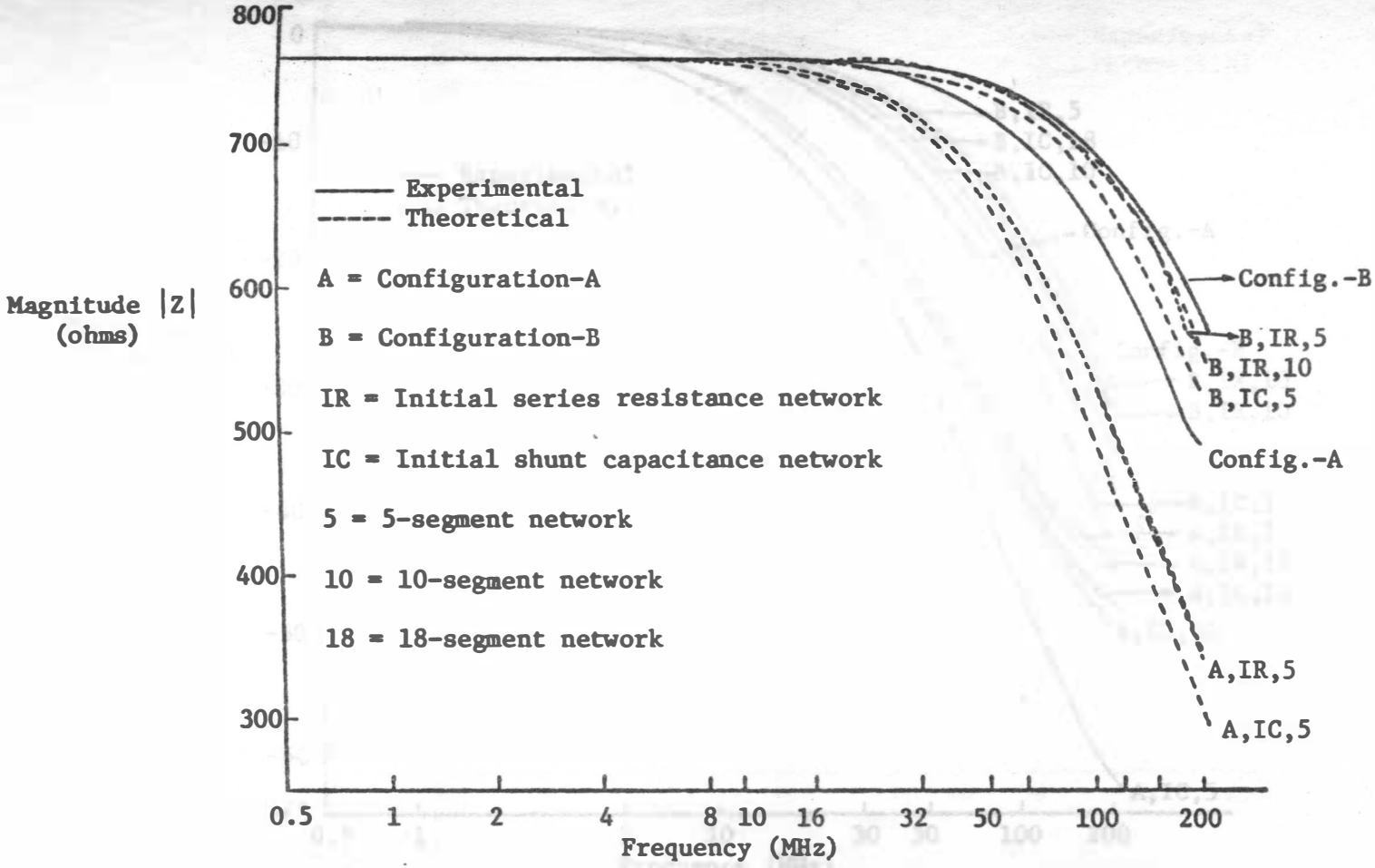



Fig. 4.10 Comparison between theoretical and observed impedance--frequency responses for 600Ω resistor.

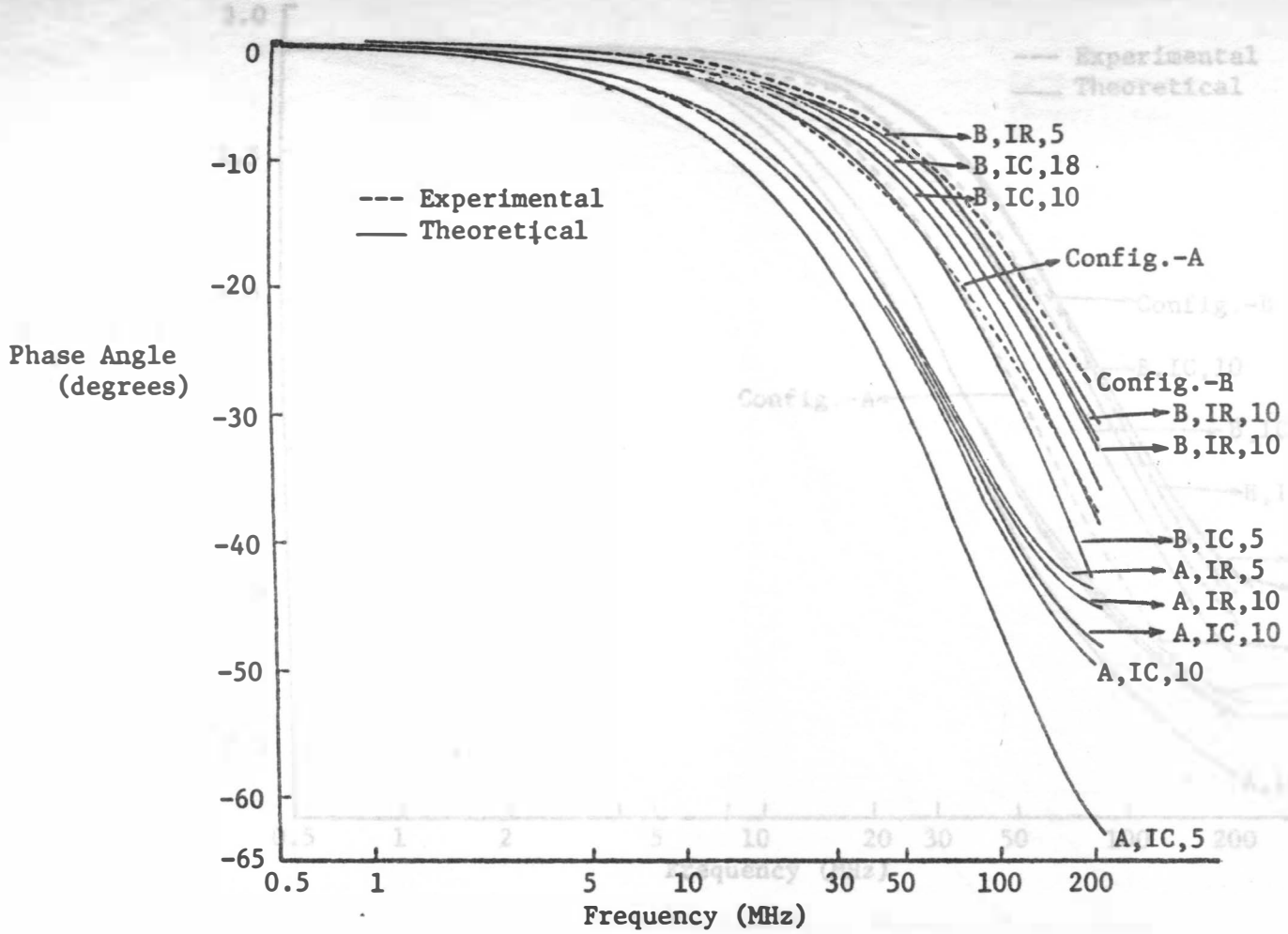



Fig. 4.11 Comparison between theoretical and observed phase angle--frequency responses for 600Ω resistor. (For notation see Fig. 4.10).

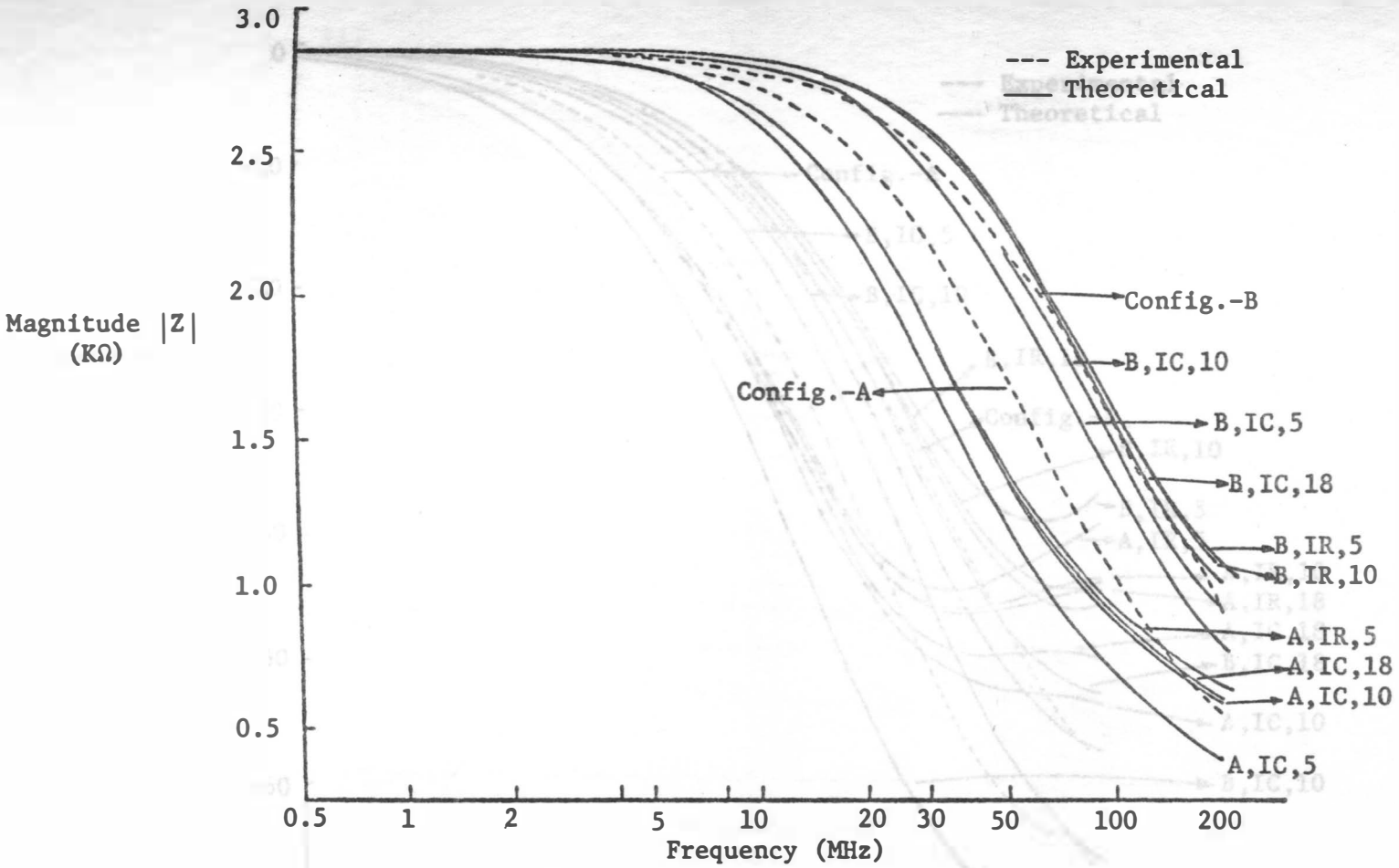



Fig. 4.12 Comparison between theoretical and observed impedance--frequency responses for 2.5KΩ resistor.
(For notation see Fig. 4.10.)

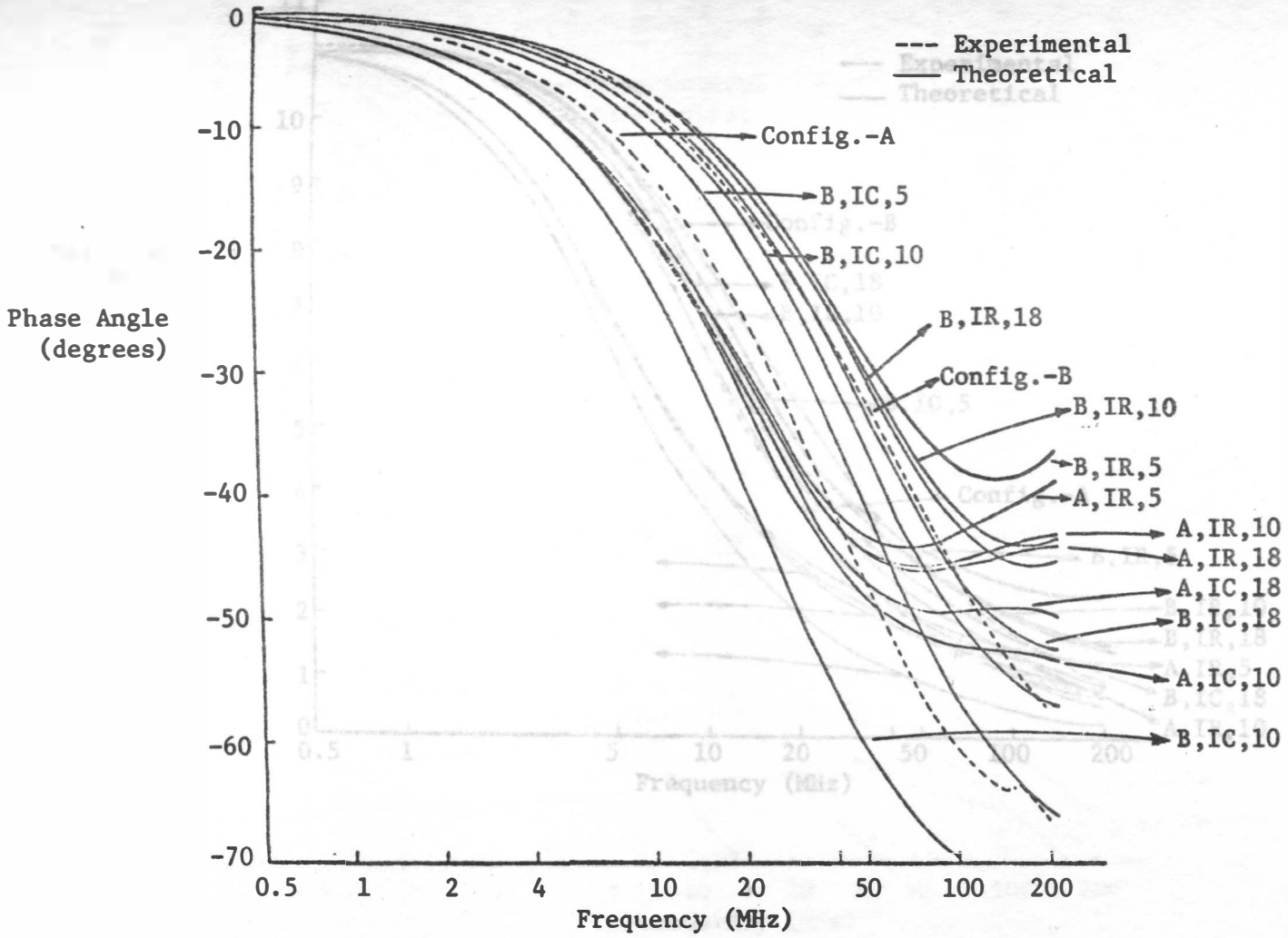



Fig. 4.13 Comparison between theoretical and observed phase angle--frequency responses for 600Ω resistor. (For notation see Fig. 4.10).

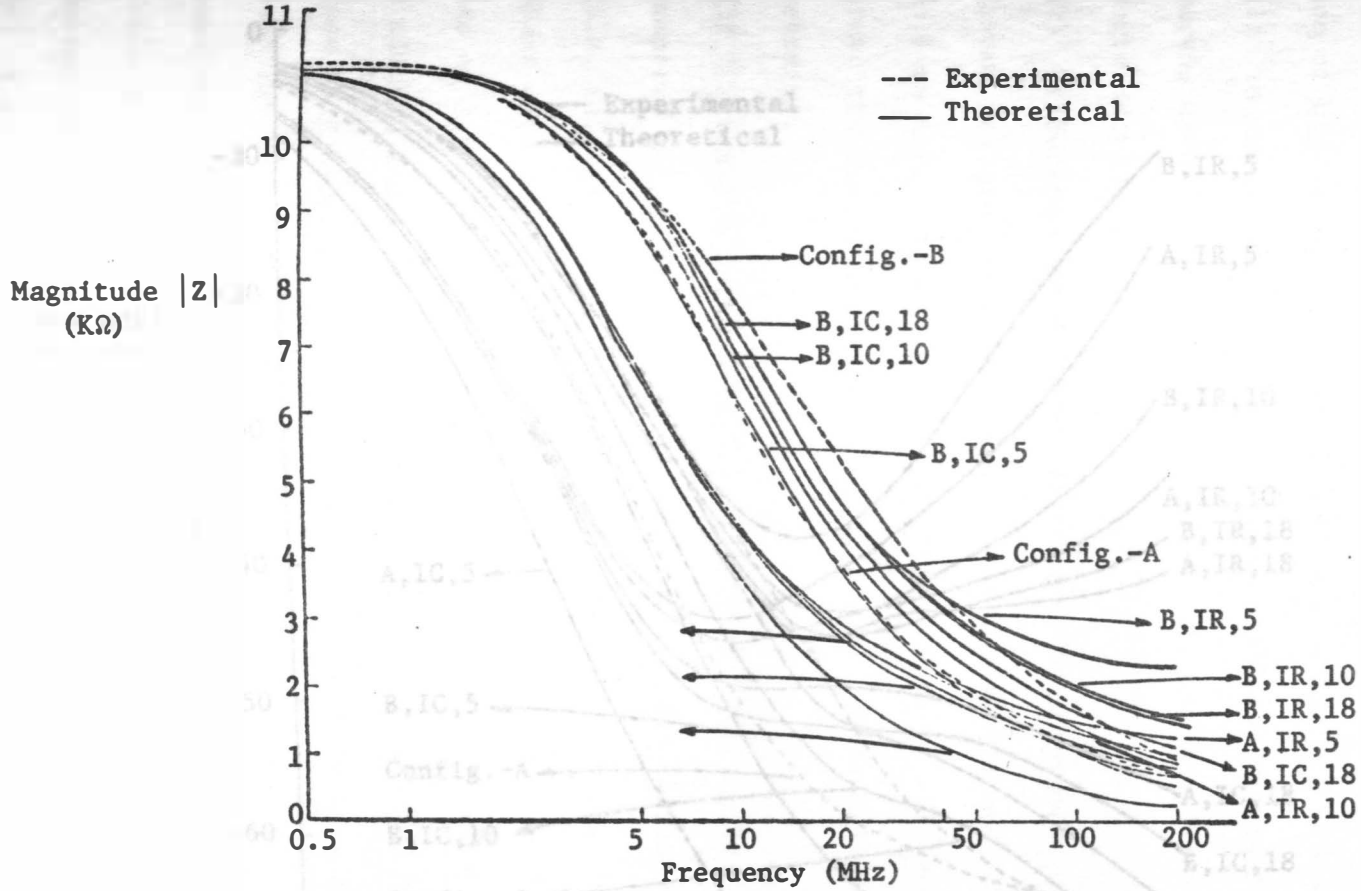



Fig. 4.14 Comparison between theoretical and observed impedance--frequency responses for 10KΩ resistor. (For notation see Fig. 4.10).

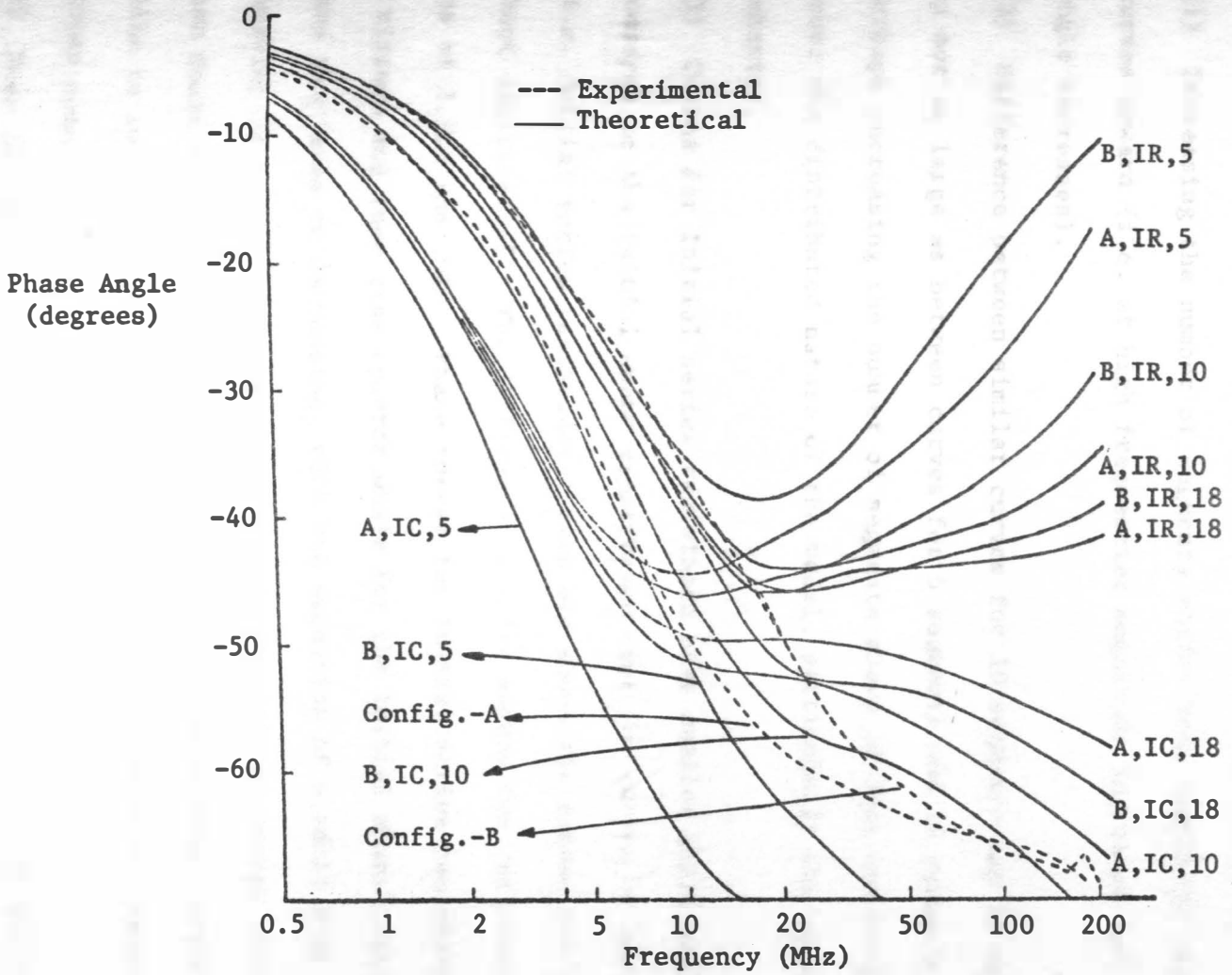



Fig. 4.15 Comparison between theoretical and observed phase angle--frequency responses for 10KΩ resistor. (For notation see Fig. 4.10).

4.3.1 Conclusions

Some of the conclusions that can be drawn on the basis of comparison of different graphs shown in Figs. 4.10 through 4.15 are:

(1) Increasing the number of segments shifts both magnitude and phase curves upward (i.e. at high frequencies magnitude increases and phase angle decreases).

(2) Difference between similar curves for 10 segments and 18 segments is not as large as between curves for 5 segments and 10 segments. Perhaps increasing the number of segments above 10 does not really improve the distributed nature of the model, particularly the magnitude behavior.

(3) Curves for initial series resistance have smaller phase angles compared to the initial shunt capacitance case for curves of same type (i.e. initial series resistance curves are above the curves for initial shunt capacitance). The difference is quite marked for resistance values of 2.5KΩ and 10KΩ. Phase curves for initial series resistance show a minimum and then rise upwards while for the initial shunt capacitance case they keep on decreasing, with the exception of a small kink. This behavior is of course expected because in the initial series resistance case there is some resistance which is not shunted across a capacitor while in initial shunt capacitance case all resistances are shunted across some capacitance.

(4) Near 200 MHz for both configurations-A and -B, (for 10 and 18 number of segments) phase angles are in the vicinity of $-60^{o}$ for resistance values of 2.5KΩ and 10KΩ.

From these conclusions it can be seen that initial shunt capacitance and 10 segment model for both configurations-A and -B, can perhaps lead to a suitable model that would fit the actual observed magnitude and phase responses closely. Further work was carried on to obtain a suitable value of capacitance that would provide a satisfactory model.

## 4.4 Substrate Resistance

After choosing the initial capacitance and 10 segment network model several different values of capacitors were tried for both configurations-A and -B for all three resistors. Comparison of theoretical and experimentally-observed responses suggests the correct direction to change the value of $C_s$ in order to obtain a better fit. If the theoretical curve is below the experimental curve then decreasing $C_s$ will move it up and hence closer to the experimentally observed response.

Since there is always some substrate resistance associated with a diffused resistor, an improved model could be considered by taking substrate resistance into account. One such distributed network composed of 10 segments with initial shunt capacitance is shown in Fig. 4.16.

To find out the effect of substrate resistance on the magnitude and phase response some additional theoretical frequency responses were obtained using ECAP.

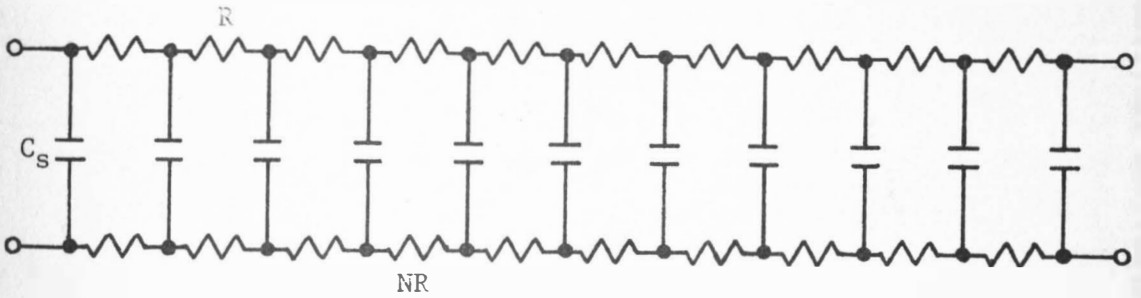



Fig. 4.16 Improved distributed RC network model for diffused resistors.

Figs. 4.17 and 4.18 show responses for configuration-A for a capacitance value of 0.5pF for the two cases of N=0.0 and N=0.1. N is the ratio of resistivity on one side of the distributed capacitance to the other side. Also shown in the figures are responses for a capacitance value of C=0.3 pF for the same two values of N.

Figs. 4.19 and 4.20 compare the response for configuration-A for capacitance value of 0.5 pF and N=0.0 and N=0.1 for 2.5KΩ resistor.

Figs. 4.21 and 4.22 compare responses for configuration-A for capacitance value of 0.9 pF and for N=0.0 and N=0.01 for 10KΩ resistor. These responses are also compared to experimental responses and to other theoretical responses in the figures.

### 4.4.1 Conclusions:

Taking substrate resistance NR into account changes the calculated response. Conclusions are:

(1) Using a value of N=0.1 or 0.01 does not affect the magnitude response very much. Magnitude responses for N=0.0 and N=0.1 are quite close.

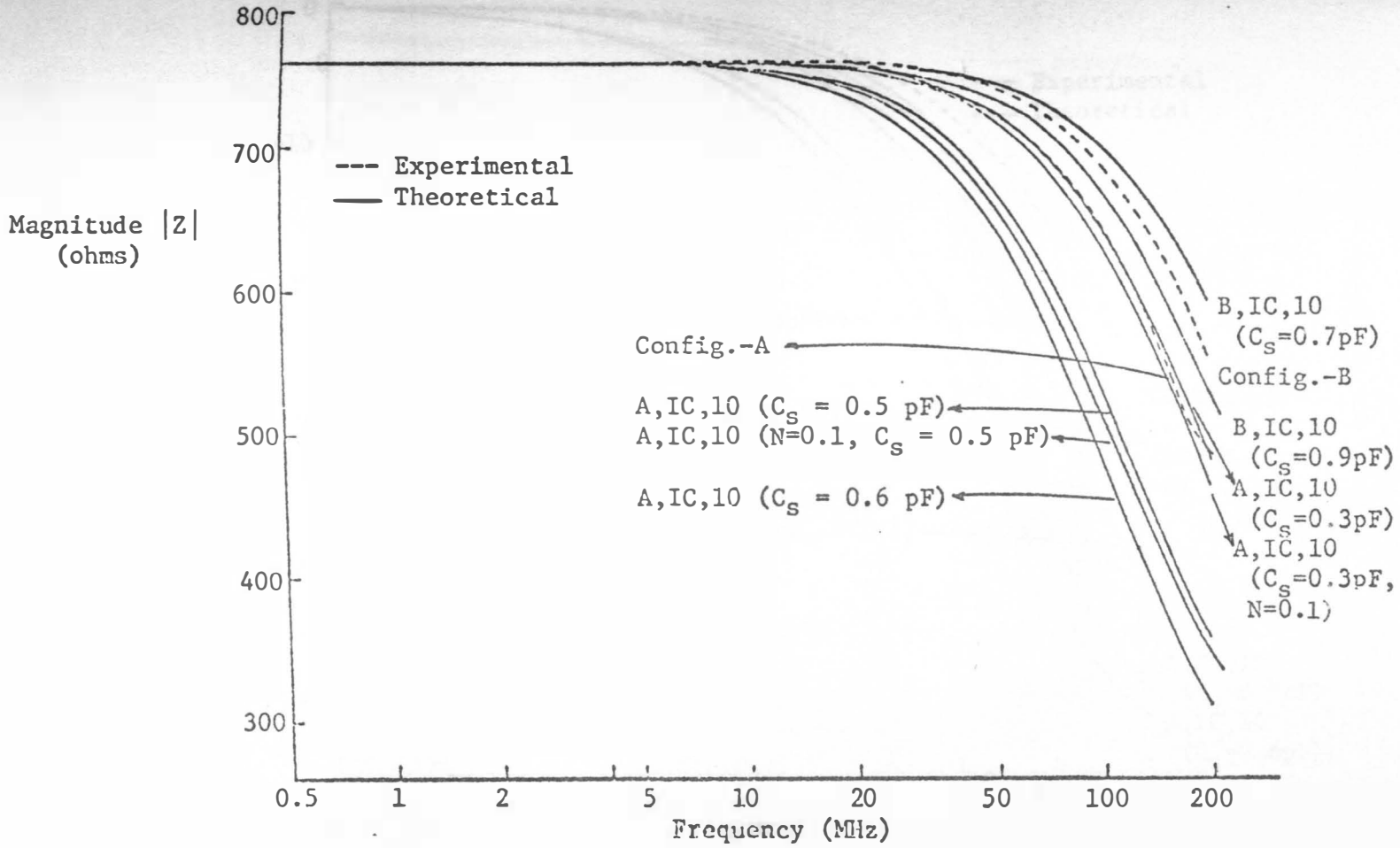



Fig. 4.17 Comparison between theoretical and observed impedance--frequency responses for 600Ω resistor to observe the effect of substrate resistance. (For notation see Fig. 4.10).

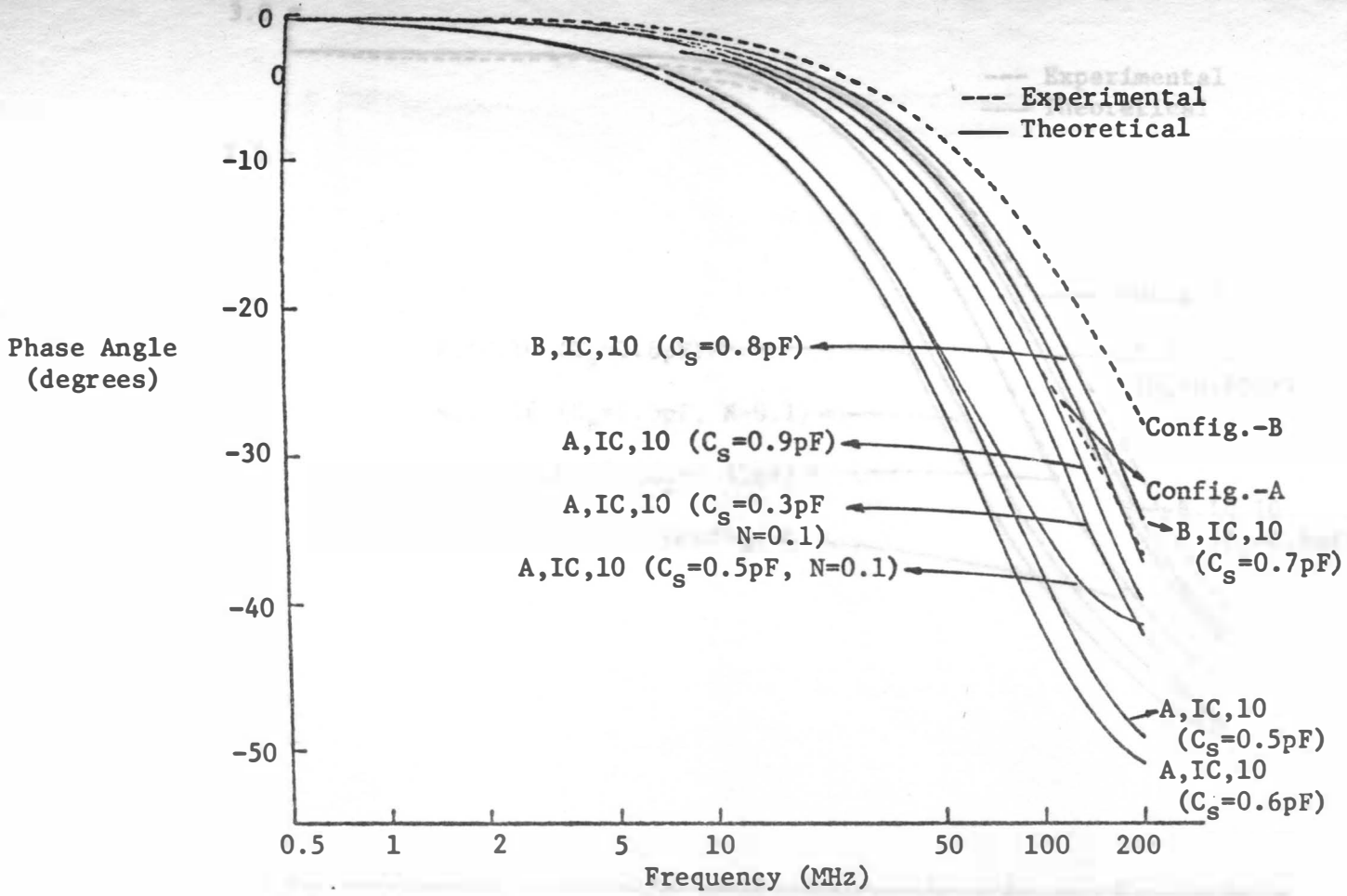



Fig. 4.18 Comparison between theoretical and observed phase angle--frequency responses for 600Ω resistor to observe the effect of substrate resistance. (For notation see Fig. 4.10)

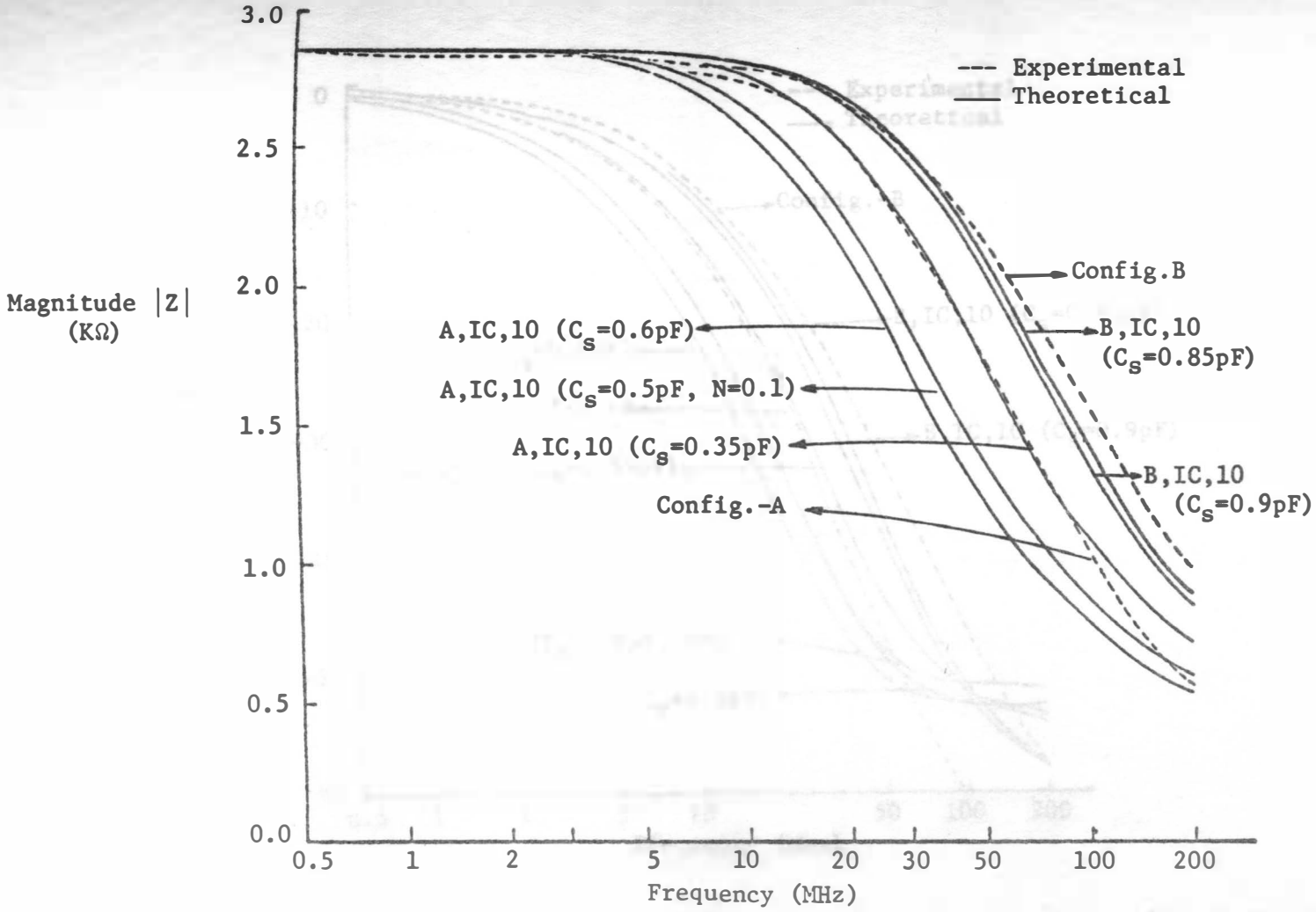



Fig. 4.19 Comparison between theoretical and observed impedance--frequency responses for 2.5KΩ resistor to observe the effect of substrate resistance. (For notation see Fig. 4.10.)

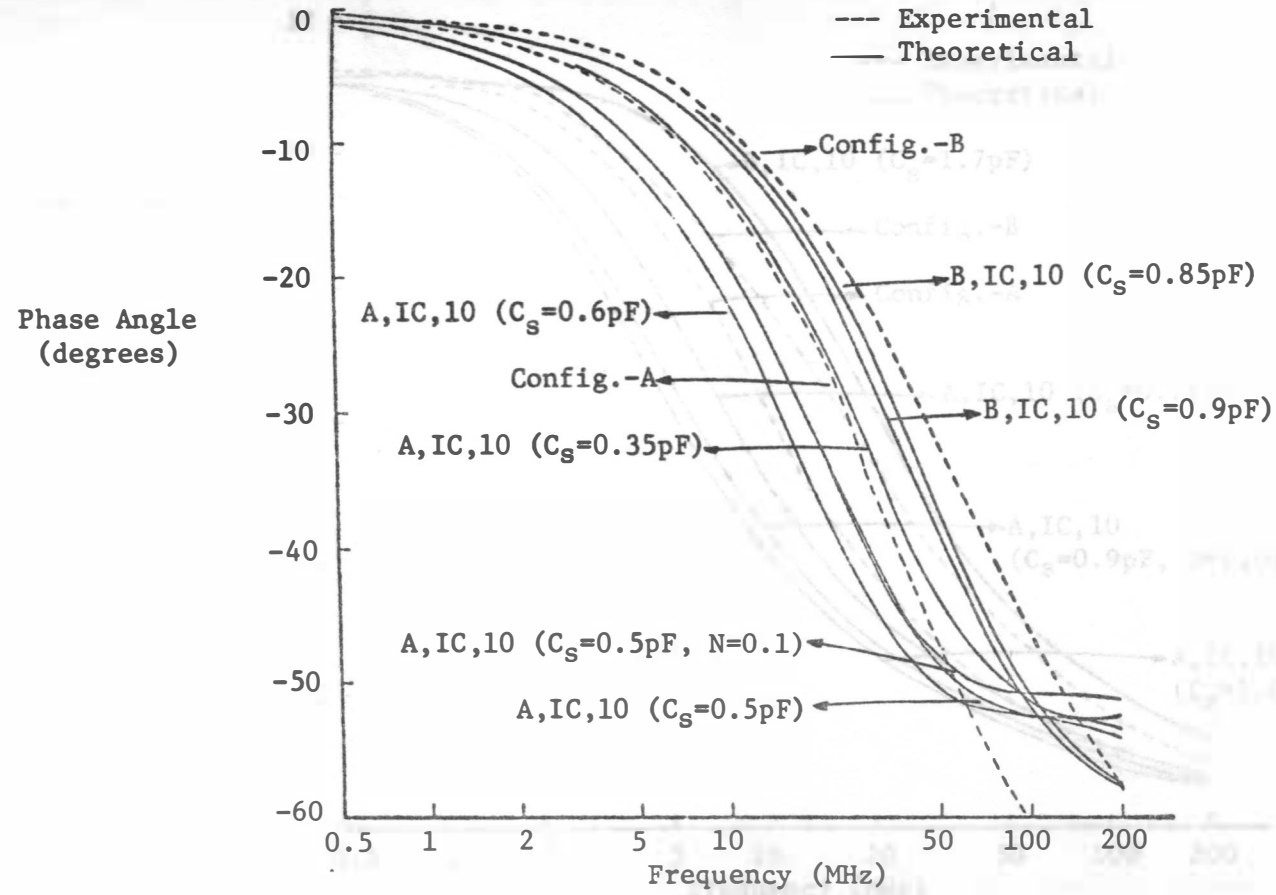



Fig. 4.20 Comparison between theoretical and observed phase angle--frequency responses for 2.5KΩ resistor to observe the effect of substrate resistance. (For notation see Fig. 4.10.)

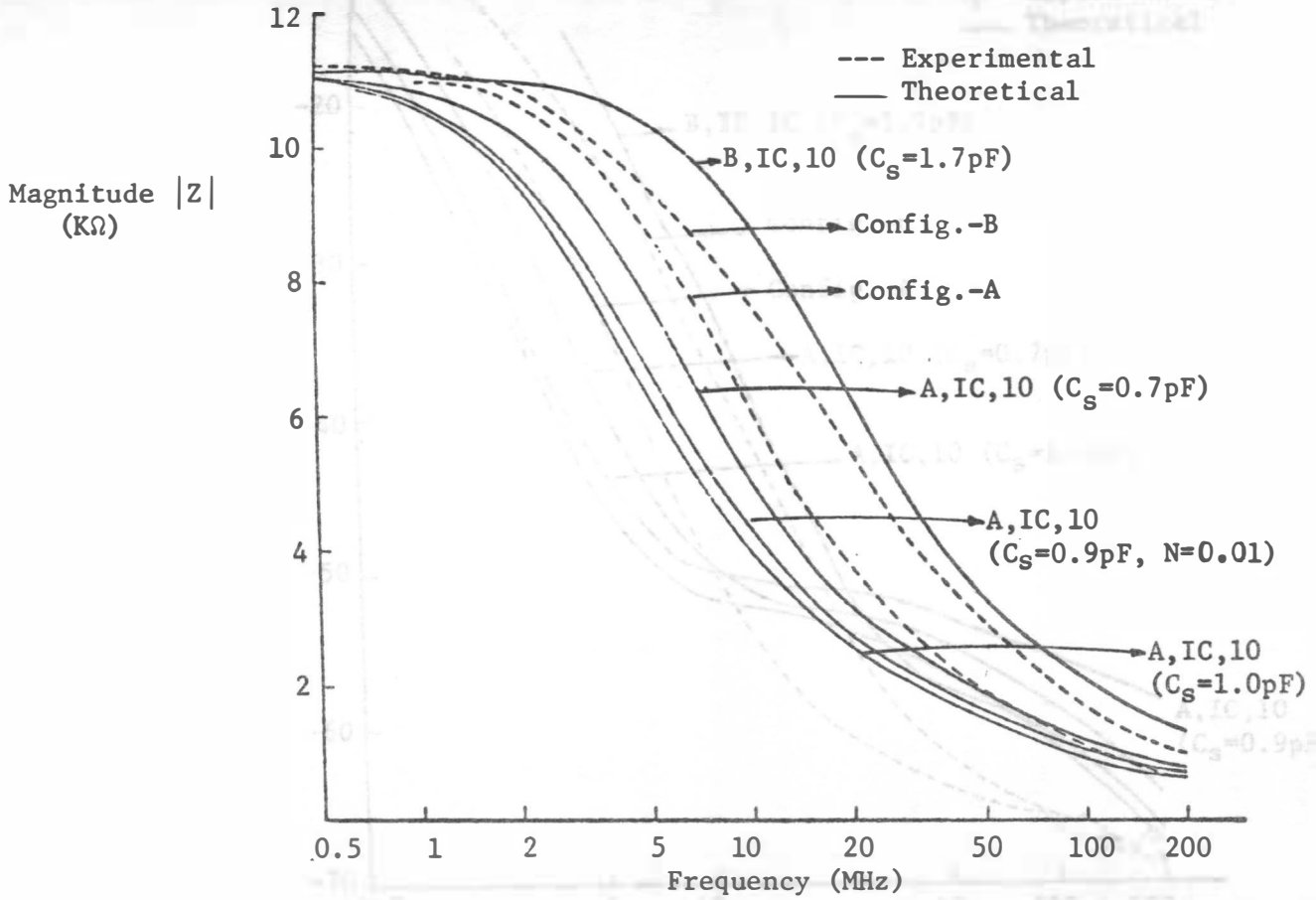



Fig. 4.21 Comparison between theoretical and observed impedance--frequency responses for 10KΩ resistor to observe the effect of substrate resistance. (For notation see Fig. 4.10.)

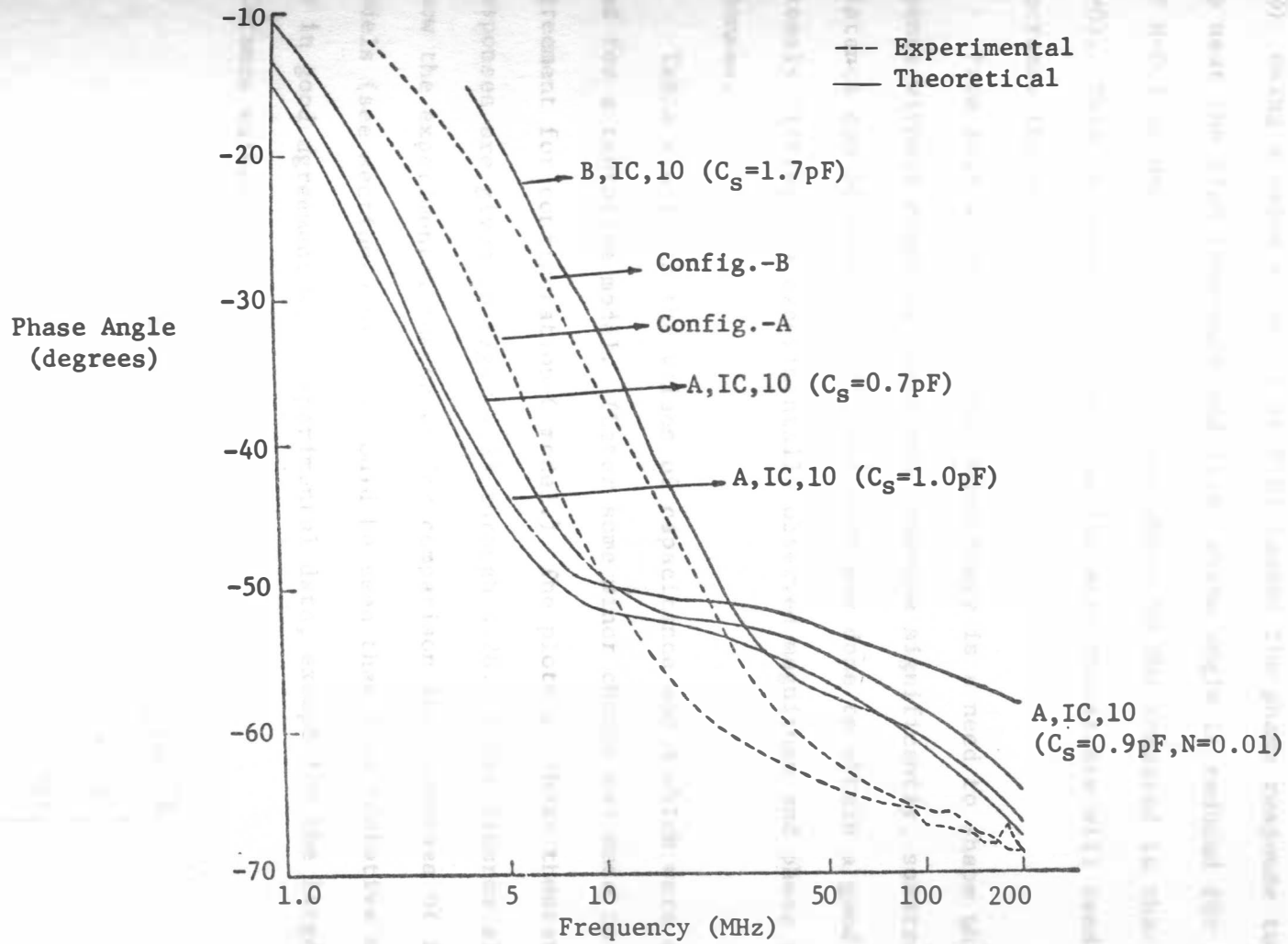



Fig. 4.22 Comparison between theoretical and observed phase angle--frequency responses for 10KΩ resistor to observe the effect of substrate resistance. (For notation see Fig. 4.10).

(2) Using a value of N=0.1 or 0.01 causes the phase response to move up near the high frequency end (i.e. phase angle is reduced for case of N=0.1 or N=0.01 for frequencies above 50 MHz compared to that for N=0). This is expected because adding more resistance will tend to decrease the phase angle.

From this we conclude that when there is a need to shape phase response without changing magnitude response significantly, substrate resistance can be used. Additional work was done to obtain a good model closely fitting the experimentally observed magnitude and phase responses.

Table 4.4 lists the values of capacitance and N which were selected for a tentative model. (Later some minor change was made to obtain agreement for configuration-C model.) The plots of these theoretical responses are given in Figs. 4.23 through 4.28. These figures also show the experimental responses for comparison and responses of final models (see section 4.8). It could be seen that this tentative model is in good agreement with experimental data, except for the larger resistance values.

| R | Configuration-A | Configuration-B |
|---|---|---|
| 600Ω | N=0.1 $C_s$=0.3pF | N=0.1 $C_s$=0.7pF |
| 2.5KΩ | N=0 $C_s$=0.35pF | N=0.1 $C_s$=0.8pF |
| 10KΩ | N=0 $C_s$=0.6pF | N=0 $C_s$=1.3pF |

Table 4.4 Values of $C_s$ and N for tentative model of resistors.

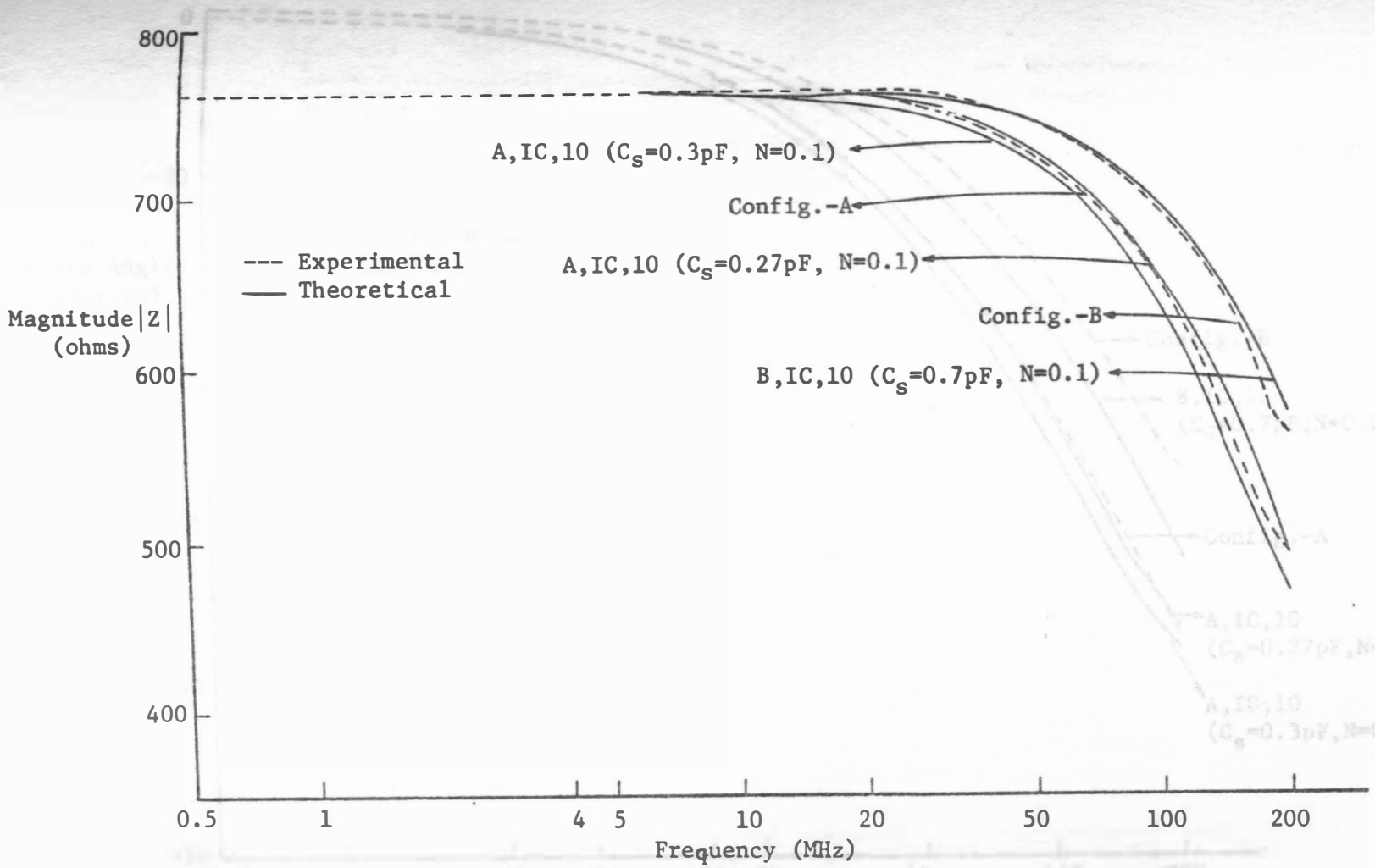



Fig. 4.23 Comparison between theoretical and observed impedance--frequency responses for 600Ω resistor resistor (final model). (For notation see Fig. 4.10).

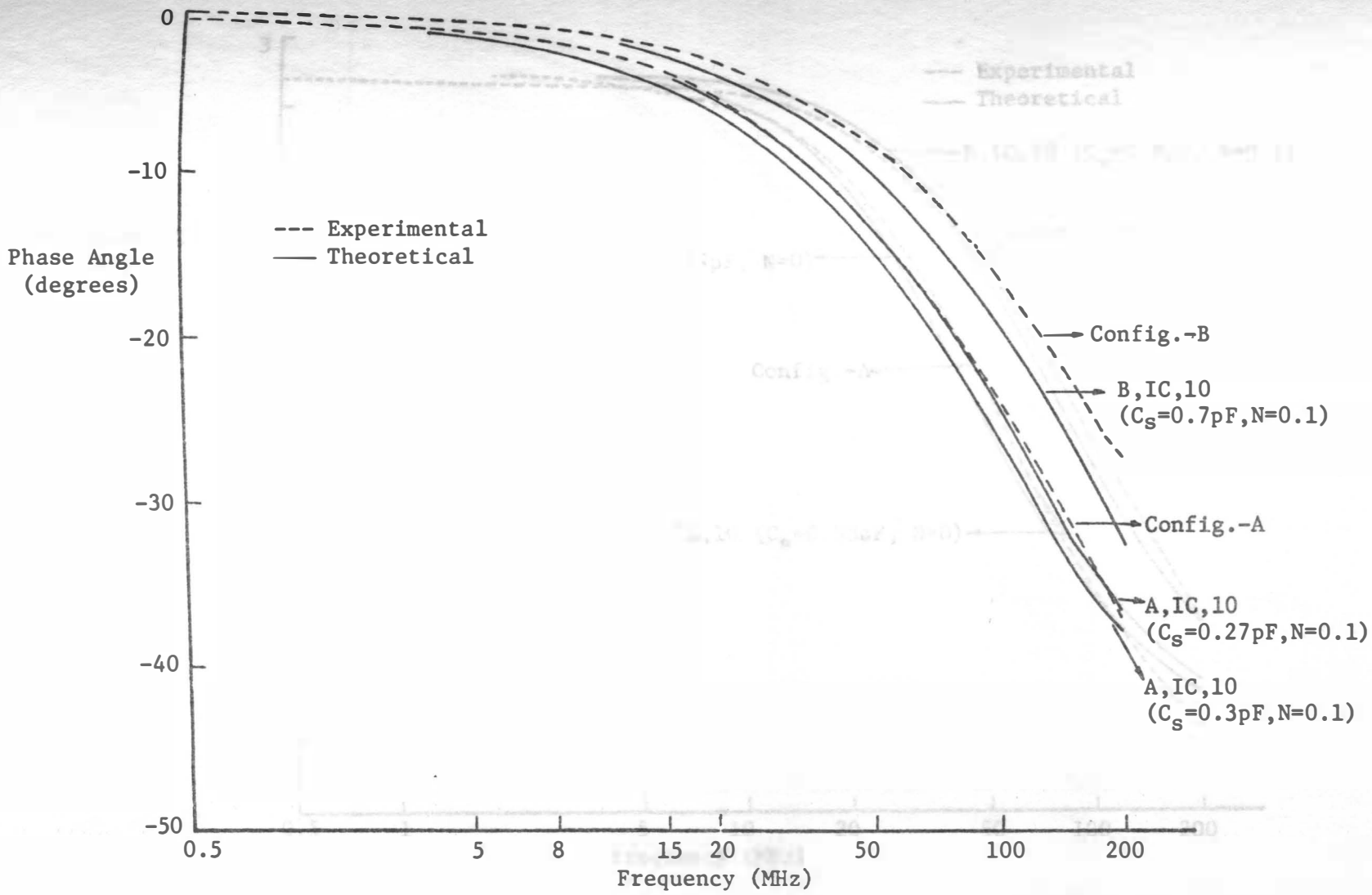



Fig. 4.24 Comparison between theoretical and observed phase angle--frequency responses for 600Ω resistor (final model). (For notation see Fig. 4.10.)

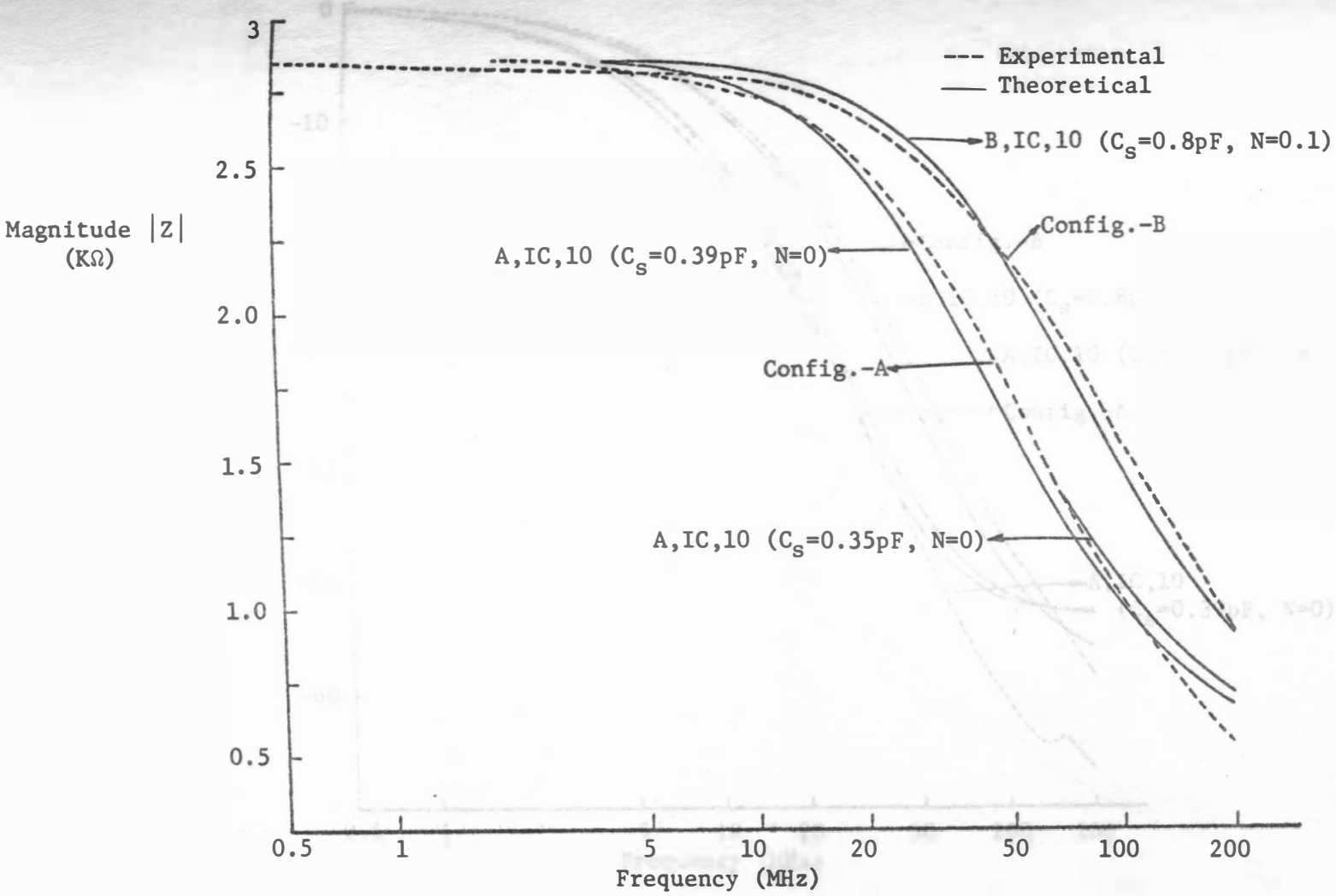



Fig. 4.25 Comparison between theoretical and observed impedance--frequency responses for 2.5KΩ resistor (final model). (For notation see Fig. 4.10.)

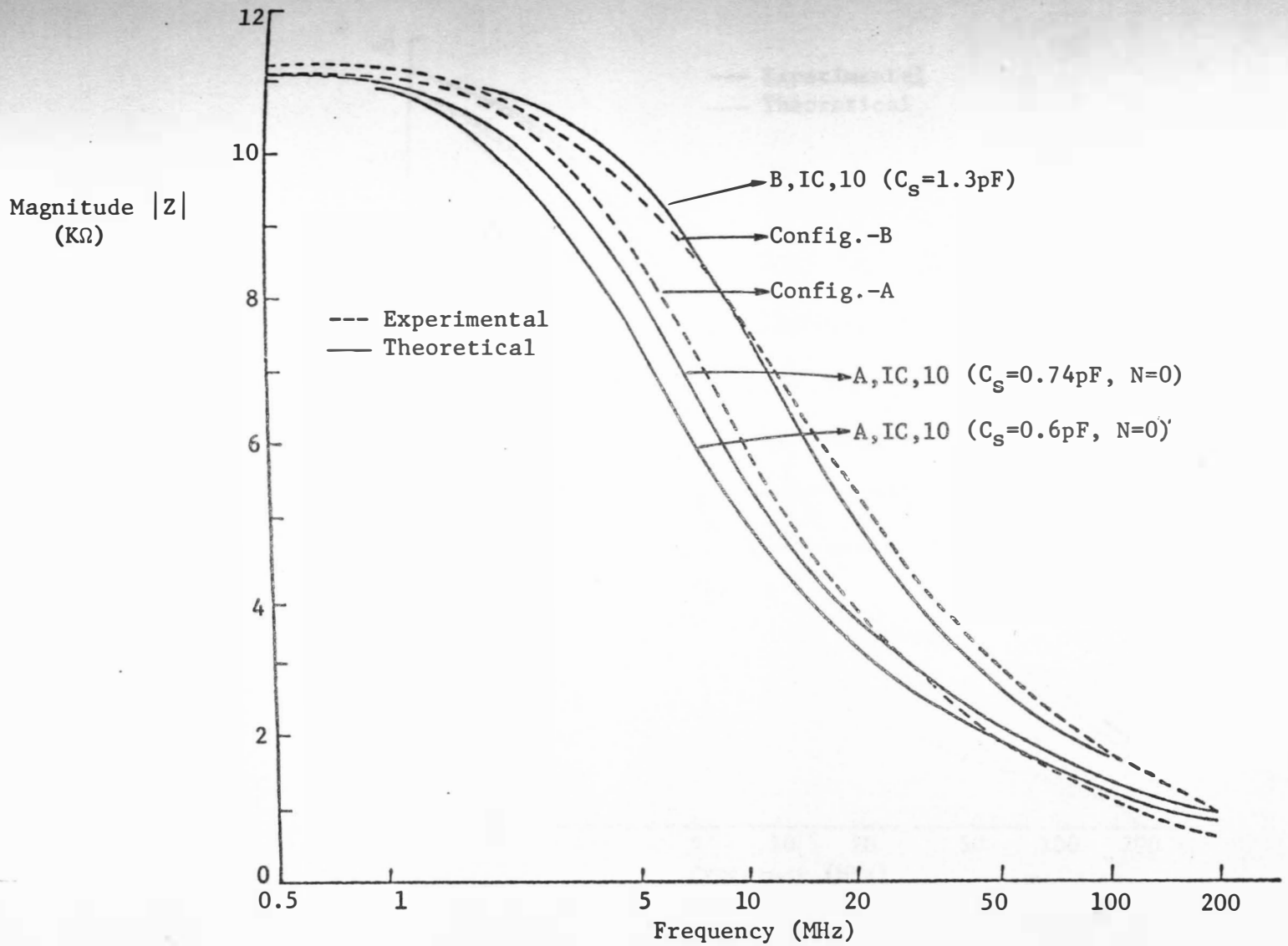



Fig. 4.27 Comparison between theoretical and observed impedance--frequency responses for 10KΩ resistor (final model). (For notation see Fig. 4.10.)

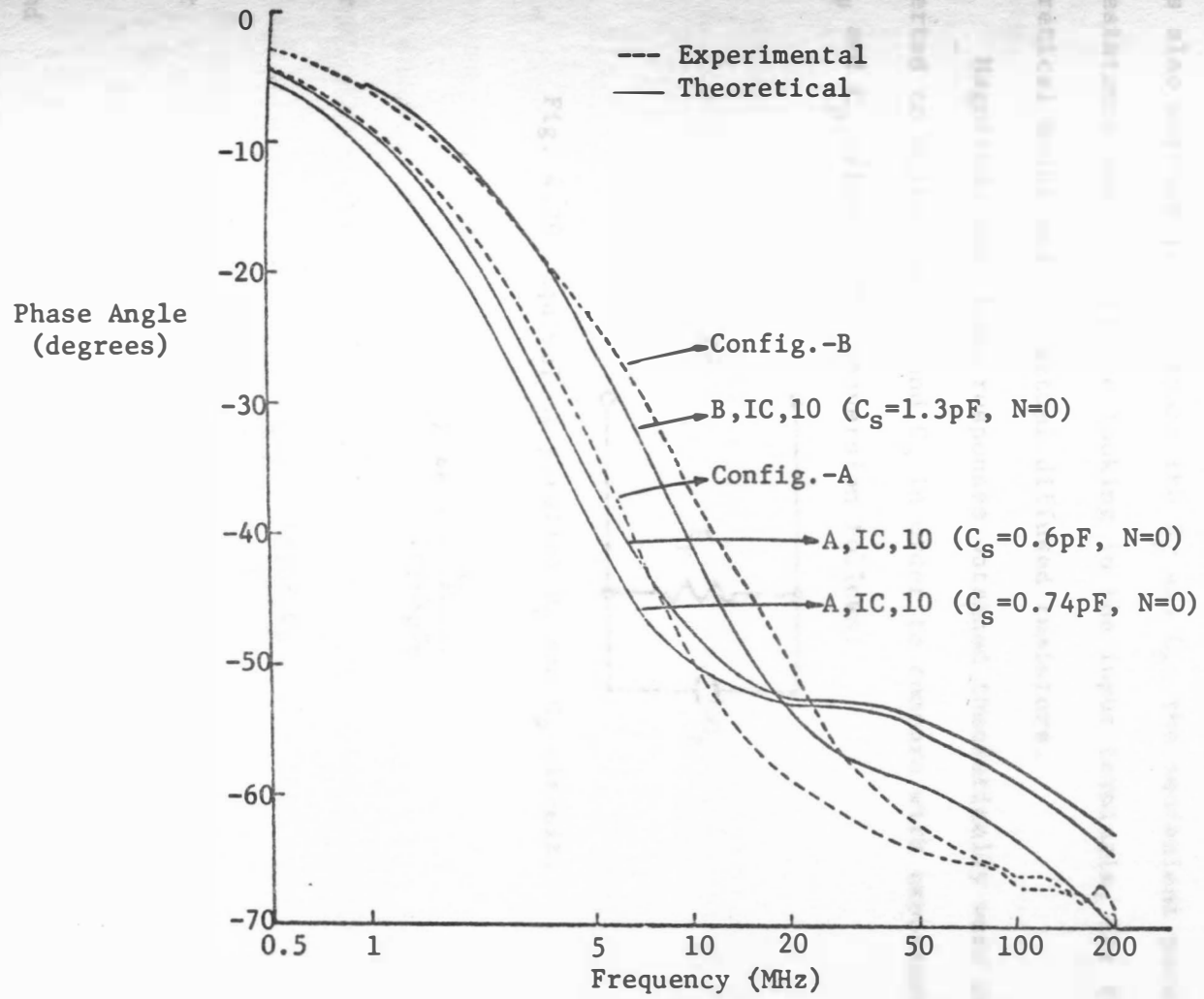



Fig. 4.28 Comparison between theoretical and observed phase angle--frequency responses for 10KΩ resistor (final model). (For notation see Fig. 4.10.)

## 4.5 Comparison of $R_p$ and $C_p$

The goal has been to obtain a good match between the observed and the theoretical impedance characteristics (magnitude and phase). It is also worthwhile to compare the $R_p$ and $C_p$, the equivalent parallel resistance and capacitance looking in the input terminals, for the theoretical model and for actual diffused resistors.

Magnitude and phase responses obtained theoretically were converted to equivalent $R_p$ and $C_p$ in order to compare with experimental $R_p$ and $C_p$ values. The conversion follows:

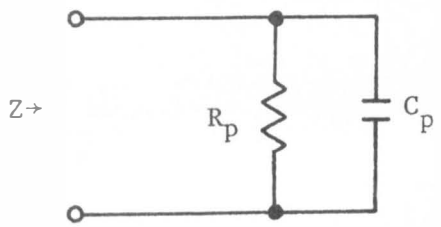



Fig. 4.29 Equivalent parallel $R_p$ and $C_p$ circuit.

$$|Z|\angle\theta = \frac{R_p}{1+j\omega R_p C_p} \tag{4.16}$$

or

$$\frac{\angle -\theta}{|Z|} = \frac{1+j\omega R_p C_p}{R_p}$$

or

$$\frac{1}{|Z|}\cos\theta = \frac{1}{R_p}$$

and

$$\frac{-\sin\theta}{|Z|} = \omega C_p \ .$$

So

$$R_p = \frac{|Z|}{\cos\theta} \tag{4.17}$$

and

$$C_p = \frac{-\sin\theta}{\omega|Z|} \tag{4.18}$$

Figs. 4.30 through 4.35 show the $R_p$ and $C_p$ plots for the theoretical model compared with the observed $R_p$ and $C_p$ for three different resistors. It can be observed that comparison is quite satisfactory. There is some deviation, of course, but the fact that the least count of the RX Meter is 0.1 pF should be kept in mind. Since the values involved are very low, order of 1-2 pF, the percentage error of 0.1 pF might seem very large.

## 4.6 Values of Sectional Capacitance

An attempt has been made to obtain a suitable model and determine the values of sectional capacitances for the model. The approach was to start with some estimated value and then modify it in the right direction based on the conclusions obtained from comparison of theoretical and observed impedance characteristics. A method could be outlined to determine the values of these sectional capacitances rather than to approach it by a trial and error basis.

### 4.6.1 Values for Configuration-A

According to Ghandhi[3] for a diffused resistor in configuration-A (or output short) the cutoff frequency $\omega_o$ is given by

$$\omega_o = \frac{2}{CR} = 2\pi f_o$$

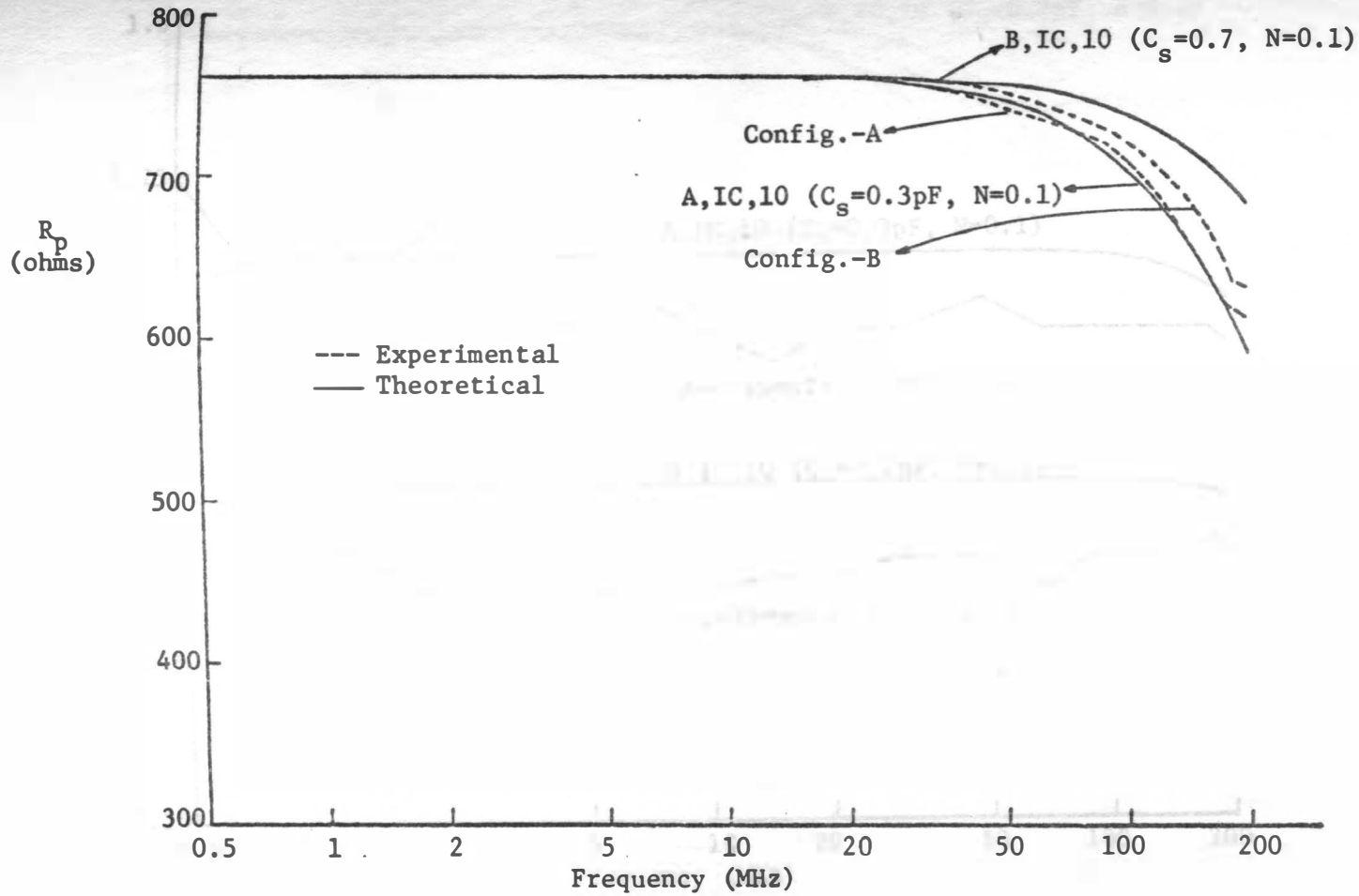



Fig. 4.30 Comparison between theoretical and observed equivalent parallel resistance--frequency responses for 600Ω resistor (tentative model). (For notation see Fig. 4.10.)

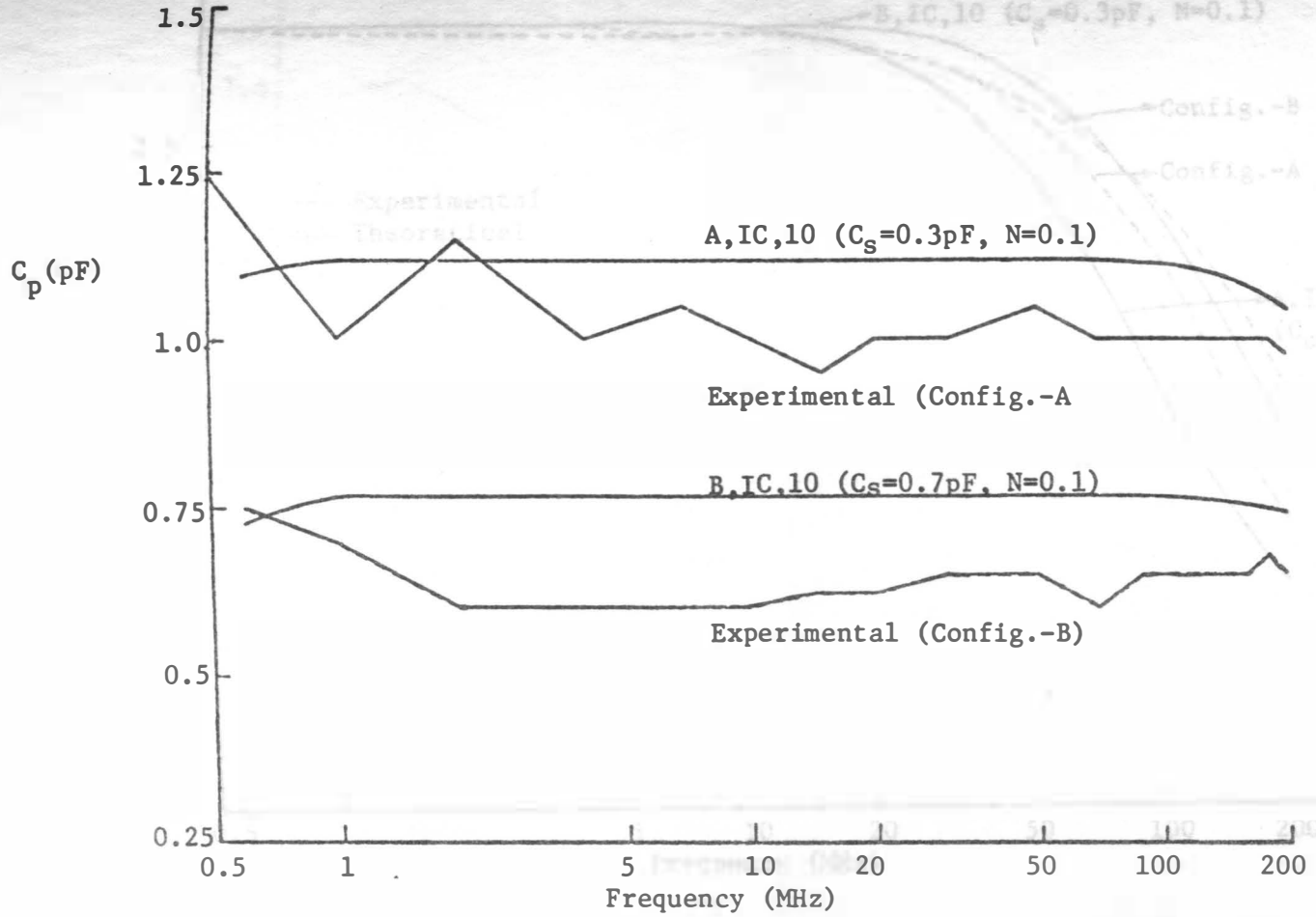



Fig. 4.31 Comparison between theoretical and observed equivalent parallel capacitance--frequency responses for 600Ω resistor (tentative model). (For notation see Fig. 4.10.)

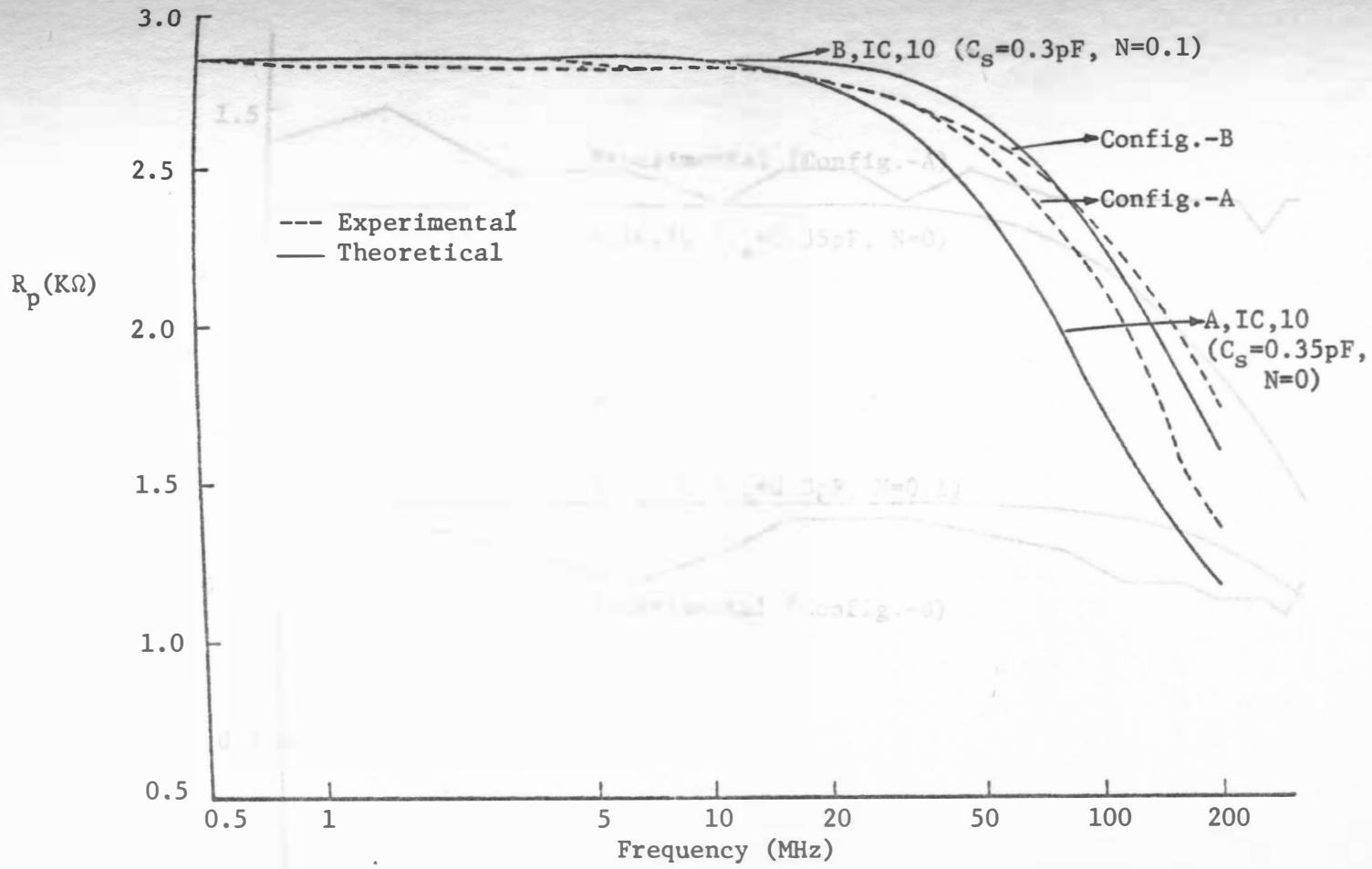



Fig. 4.32 Comparison between theoretical and observed equivalent parallel resistance--frequency responses for 2.5KΩ resistor (tentative model). (For notation see Fig. 4.10.)

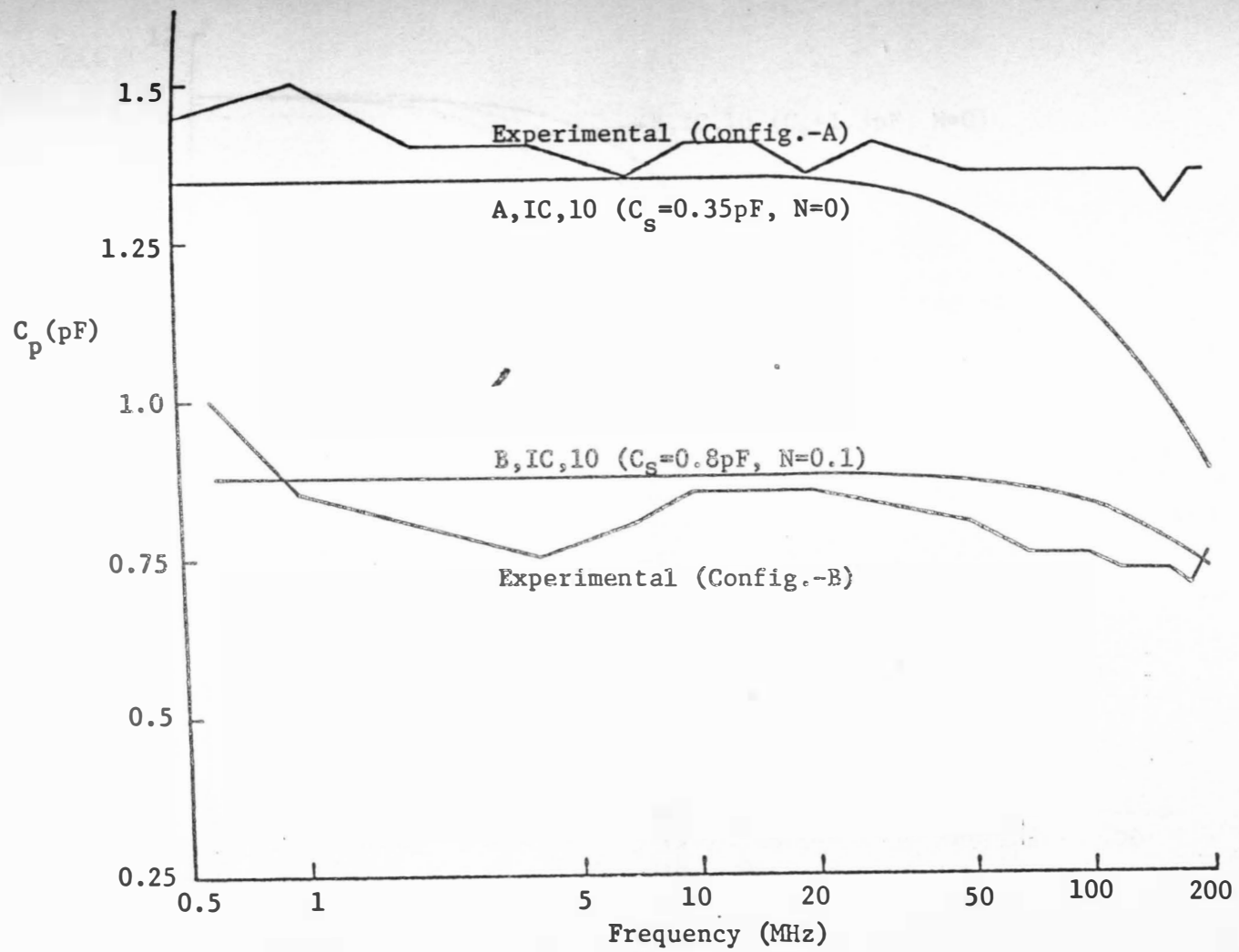



Fig. 4.33 Comparison between theoretical and observed equivalent parallel capacitance--frequency responses for 2.5KΩ resistor (tentative model). (For notation see Fig. 4.10.)

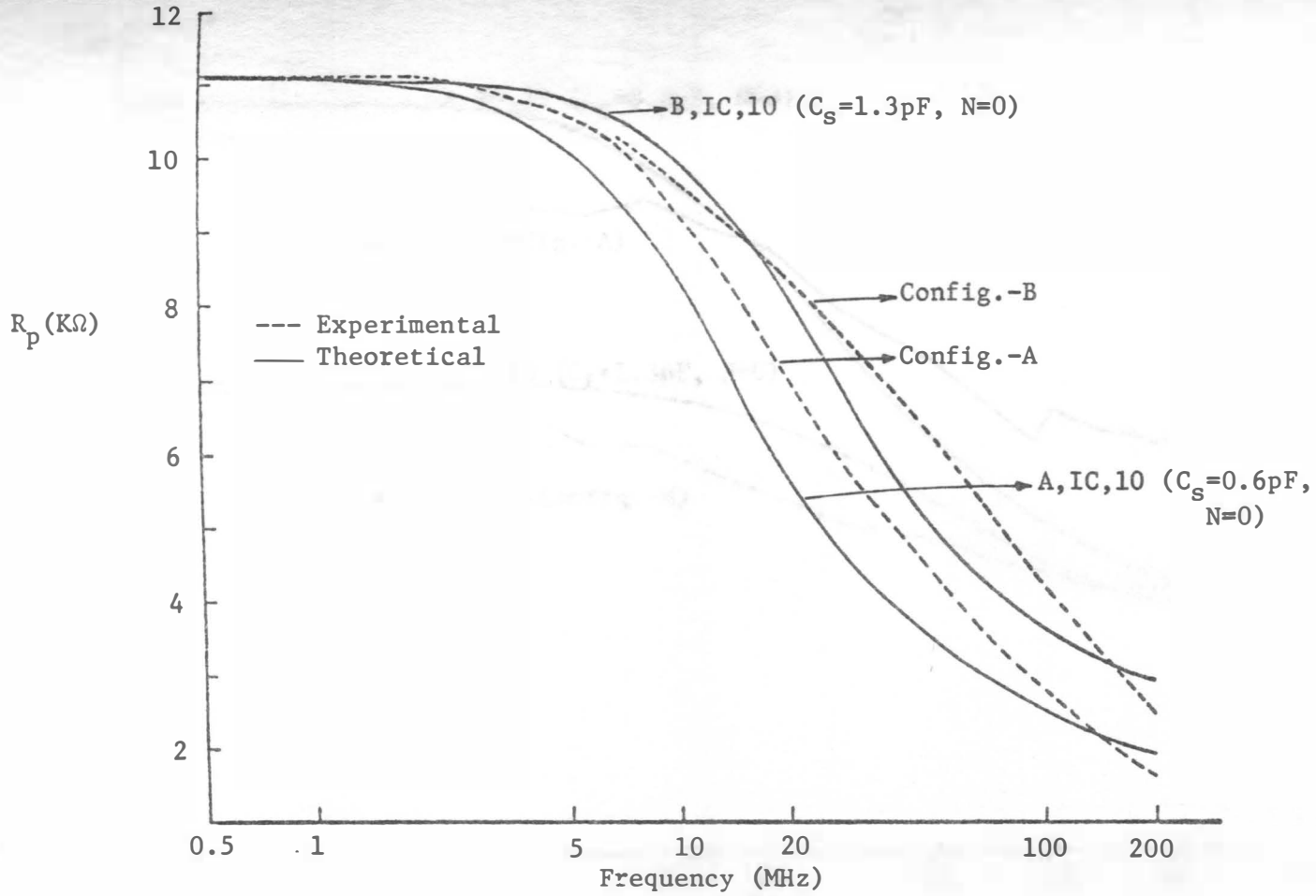



Fig. 4.34 Comparison between theoretical and observed equivalent parallel resistance--frequency responses for 10KΩ resistor (tentative model). (For notation see Fig. 4.10.)

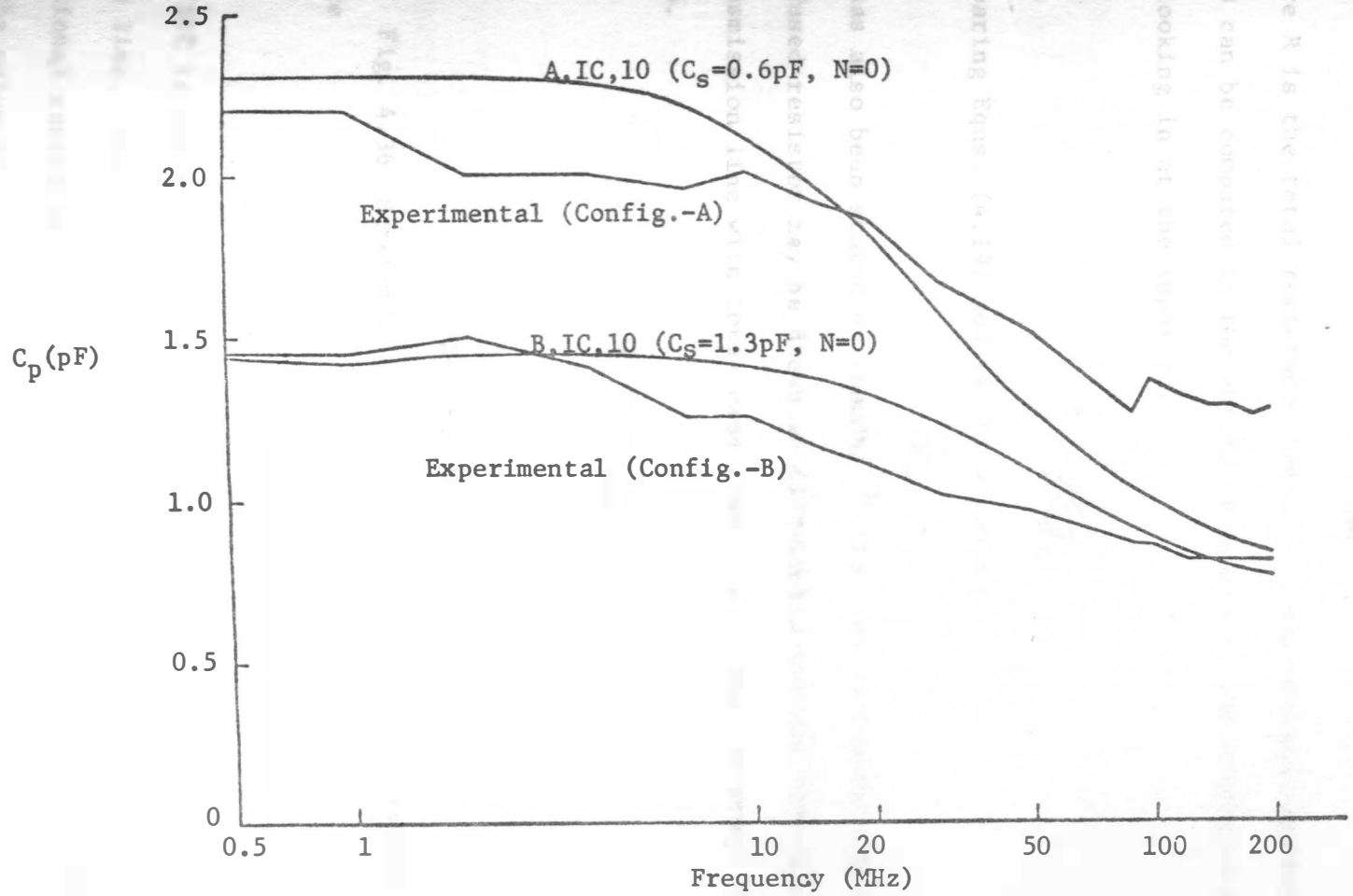



Fig. 4.35 Comparison between theoretical and observed equivalent parallel capacitance--frequency responses for 10KΩ resistor (tentative model). (For notation see Fig. 4.10.)

or

$$f_o = \frac{1}{\pi RC} \tag{4.19}$$

where R is the total resistance and $\bar{C}$ is total average capacitance. This can be compared to the cutoff frequency of the effective $R_p$ and $C_p$ looking in at the input port.

$$f = \frac{1}{2\pi R_p C_p} \tag{4.20}$$

Comparing Eqns. (4.19) and (4.20) we obtain

$$2C_p = \bar{C} \tag{4.21}$$

It has also been stated by Ghandhi[3] that the equivalent circuit of a diffused resistor may be drawn in distributed network form as an RC transmission line with total capacitance of $(\pi^2/8)\bar{C}$ as shown in Fig. 4.36.

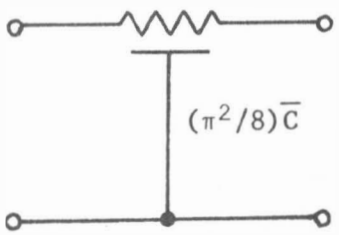



Fig. 4.36 Schematic representation of a diffused resistor.

Hence

$$\left(\frac{\pi^2}{8}\right)\bar{C} = \left(\frac{\pi^2}{8}\right)2C_p = \frac{\pi^2}{4} \cdot C_p$$

$(\pi^2/8)\bar{C}$ is the total capacitance that exists in a distributed transmission line. The model that was developed for configuration-A had eleven sectional capacitances. Hence the total capacitance is $11C_s$ where $C_s$ is the value of each sectional capacitance. Equating the total capaci-

tance $\pi^2/8(\bar{C})$ (or $\pi^2/4\ C_p$) of a distributed transmission line to the total capacitance $11C_s$ in a theoretical model, we have

$$11C_s = \frac{\pi^2}{4} C_p \quad \text{or} \quad C_s = \frac{\pi^2}{4} \cdot \frac{C_p}{11} = 0.228\ C_p \qquad (4.22)$$

Here a note is important about $C_p$. The $C_p$ used in the above expression is the value of equivalent parallel capacitance $C_p$ measured at 0.5 MHz. This can be explained as follows. At 0.5 MHz the impedance of a 1-2 pF capacitor is very high. (There was no other instrument with which capacitances of order of 1-2 pF could be measured with accuracy below 0.5 MHz.) With this high impedance we can neglect series resistances. Perhaps, to a very crude approximation, the network can be considered as just a parallel combination of 11 sectional capacitances providing a total capacitance looking in of $11C_s$.

Hence, from Eqn. (4.22), the sectional value of capacitance $C_s$ can be determined. Table 4.5 lists the values of $C_p$ at 0.5 MHz, $C_s$ obtained from Eqn. (4.22) and actual values of $C_s$ used in the final theoretical model.

| R | $C_p$(0.5MHz) | $C_s$ from Eqn. (4.22) = 0.228 $C_p$ | Actual $C_s$ used |
|---|---|---|---|
| 600Ω | 1.25 pF | 0.285 pF | 0.3 pF |
| 2.5KΩ | 1.45 pF | 0.331 pF | 0.35 pF |
| 10KΩ | 2.2 pF | 0.5 pF | 0.6 pF |

Table 4.5 Comparison of actual and theoretically calculated $C_s$ values (configuration-A).

It can be seen that values of $C_s$ obtained from Eqn. (4.22) for configuration-A are quite close to the theoretical models that were found to fit well with the actual observed responses.

### 4.6.2 Values for Configuration-B

Table 4.6 compares the measured values of equivalent parallel capacitance $C_p$ at 0.5 MHz to the values of sectional capacitance $C_s$ used in the final model accepted for the diffused resistors.

| R | $C_p$(0.5MHz) | Actual $C_s$ used |
|---|---|---|
| 600Ω | 0.75 pF | 0.7 pF |
| 2.5KΩ | 1.0 pF | 0.8 pF |
| 10KΩ | 1.45 pF | 1.3 pF |

Table 4.6 Comparison of $C_p$ and actual $C_s$ used in the model (configuration-B).

From the above discussion it can be concluded that from measurements it is possible to arrive at values for $C_s$ that will give a good start and will lead to an acceptable theoretical model for configuration-B. Perhaps a more complex model could be devised but here only a rather simple model was considered.

## 4.7 Comparison of 0.707 points for Configuration-A

Table 4.7 lists the actual 0.707 points observed from experimentally observed magnitude responses. It also lists the cutoff points calculated from the actual values of $C_s$ which were used in the tentative model. The following gives the way to obtain $f_{co}$ from $C_s$:

$$\text{Total Capacitance} = 11C_s = \frac{\pi^2}{8} \cdot \bar{C}$$

or

$$\bar{C} = \frac{11C_s}{\frac{\pi^2}{8}} = \frac{88}{\pi^2} C_s \simeq 8.8\ C_s \qquad (4.23)$$

Therefore

$$f_{co} = \frac{1}{\pi R \bar{C}} \qquad (4.24)$$

| R | Frequency for observed 0.707 point | Frequency for calculated 0.707 point |
|---|---|---|
| 600Ω | 165 MHz | 158.5 MHz |
| 2.5KΩ | 35 MHz | 36.2 MHz |
| 10KΩ | 5.2 MHz | 5.45 MHz |

Table 4.7 Comparison of observed and calculated frequencies corresponding to 0.707 magnitude points (configuration-A).

It can be seen that 0.707 points compare quite well.

An additional support to the theoretical models obtained so far was given by applying the model for configuration-A to configuration-C with proper modifications, and comparing predicted behavior with the observed responses. The next section discusses this in detail.

## 4.8 Configuration-C

Configuration-C, as described before, is the configuration in which output port is in open circuit. Since a model has already been established for configuration-A which differs from the configuration-C model only in the respect that in former output port is short-circuited, it is expected that the same model would be applicable to configuration-C

with output port open. The model established for configuration-A predicts the impedance characteristics of actual diffused resistors closely. It is possible that the same model in configuration-C might not predict the characteristics for configuration-C closely. But the validity of the same model for configuration-C would show the model to be a good representation of diffused resistor.

If the ten segment initial shunt capacitance model shown in Fig. 4.37 is considered, at 0.5 MHz the capacitance looking in at the input port with output port open will be, to a crude approximation, the sum of all sectional capacitances.

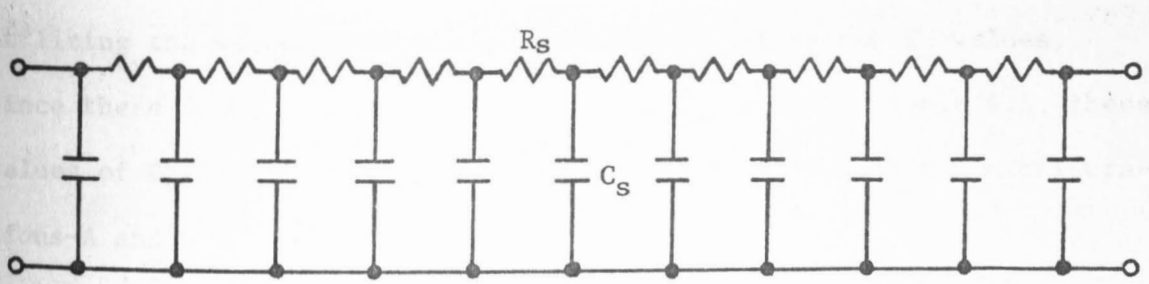



Fig. 4.37 10 segment, initial shunt capacitance model for configuration-C.

Because there are 11 sectional capacitances used in the model, it can be expected that $C_p$ at 0.5 MHz would equal $11C_s$. Table 4.8 lists the experimental $C_p$ observed at 0.5 MHz for configuration-C and also $C_p/11$. This also has been compared to the values of $C_s$ which were actually used in the tentative model obtained for configuration-A. It can be seen in fact $C_p/11$ and $C_s$ are nearly equal.

It was considered useful to obtain the magnitude and phase responses for configuration-A, using the values of capacitance as listed under $C_p/11$ column in Table 4.8 and compare them with the observed

| R | $C_p$(0.5 MHz) | $\frac{C_p}{11}$ | $C_s$(configuration-A) |
|---|---|---|---|
| 600Ω | 3.05 pF | 0.27 pF | 0.3 pF |
| 2.5KΩ | 4.3 pF | 0.39 pF | 0.35 pF |
| 10KΩ | 7.7 pF | 0.7 pF | 0.6 pF |

Table 4.8 $C_s$ and experimentally observed $C_p$ values for configuration-C.

responses as shown in Figs. 4.23 through 4.28. These theoretical responses match more closely (to the observed ones) than the tentative model responses (see Table 4.4). Table 4.9 compares the frequency corresponding to 0.707 points and the values of $C_s$ with those obtained utilizing the values of $C_p/11$ given in Table 4.8 as new $C_s$ values. Since these compare nearly as well as for $C_s$ values of Table 4.4, these values of $C_p/11$ can be selected as final model $C_s$ values for configurations-A and -C.

| R | $C_s$ values using Eqn.(4.22) | New $C_s$ values | Frequency corresponding 0.707 point | Cutoff frequency using Eqn.(4.24) |
|---|---|---|---|---|
| 600Ω | 0.285 pF | 0.27 pF | 165 MHz | 176 MHz |
| 2.5KΩ | 0.33 pF | 0.39 pF | 35 MHz | 32.6 MHz |
| 10KΩ | 0.5 pF | 0.74 pF | 5.2 MHz | 4.5 MHz |

Table 4.9 Comparison of cutoff frequencies and $C_s$ values for configuration-A (final model).

Figs. 4.38 and 4.39 show the magnitude and phase responses (obtained from theoretical model with values as given under the $C_p/11$ column in Table 4.8) compared against the experimentally observed responses.

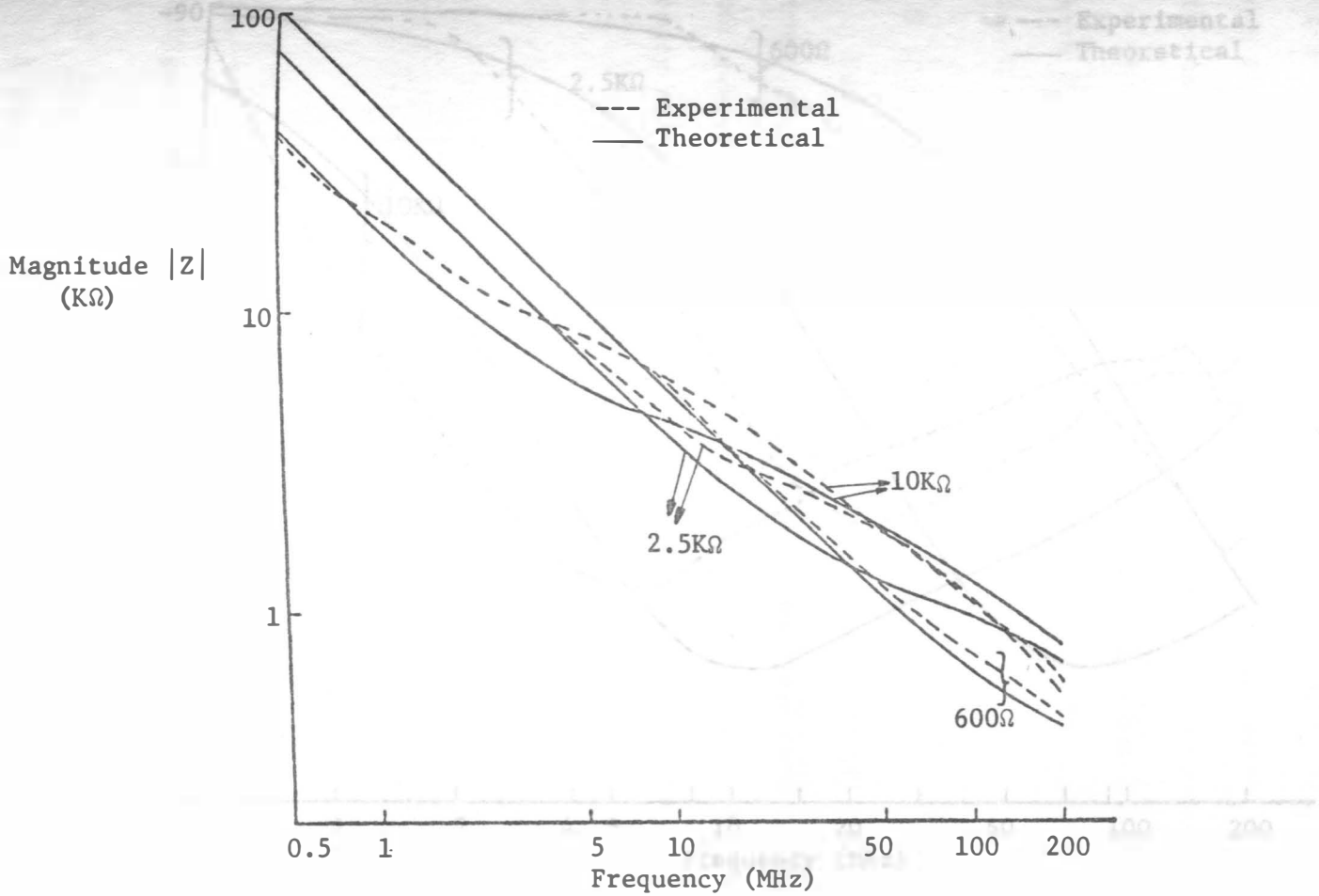



Fig. 4.38 Comparison between theoretical and observed impedance--frequency responses for configuration-C.

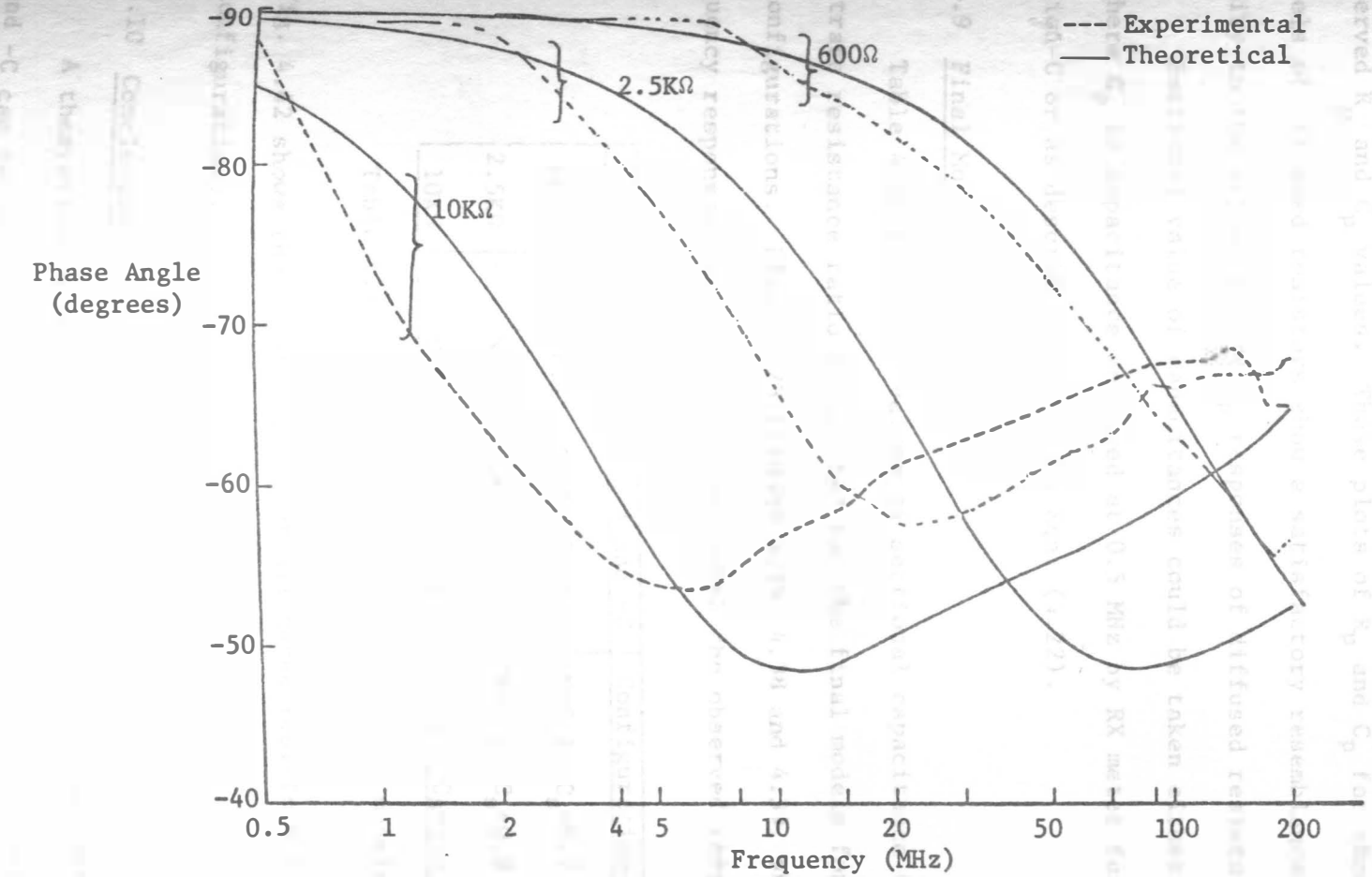



Fig. 4.39 Comparison between theoretical and observed phase angle--frequency responses for configuration-C.

Figs. 4.40 and 4.41 also compare the $R_p$ and $C_p$ for the same models (as used for Figs. 4.38 and 4.39) with the experimentally observed $R_p$ and $C_p$ values. These plots of $R_p$ and $C_p$ for theoretical models of diffused resistors show a satisfactory resemblance and proximity to the actual $R_p$ and $C_p$ responses of diffused resistors.

Sectional value of capacitances could be taken either from $C_p/11$ where $C_p$ is capacitance measured at 0.5 MHz by RX meter for configuration-C or as described earlier by Eqn. (4.22).

## 4.9 Final Models

Table 4.10 lists the values of sectional capacitance $C_s$ and substrate resistance ratio N accepted for the final models for different configurations. Figs. 4.23 through 4.28, 4.38 and 4.39, show the frequency responses for these, compared with the observed responses.

| R | Configurations-A and -C | Configuration-B |
|---|---|---|
| 600Ω | N=0.1 $C_s$=0.27 pF | N=0.1 $C_s$=0.7 pF |
| 2.5KΩ | N=0 $C_s$=0.39 pF | N=0.1 $C_s$=0.8 pF |
| 10KΩ | N=0 $C_s$=0.74 pF | N=0 $C_s$=1.3 pF |

Table 4.10 Values of $C_s$ and N for final models.

Fig. 4.42 shows the final models for all three resistors for all three configurations.

## 4.10 Conclusions

A theoretical model fitting diffused resistors in configurations-A and -C can be obtained (see Figs. 3.3 and 3.5). This model predicts

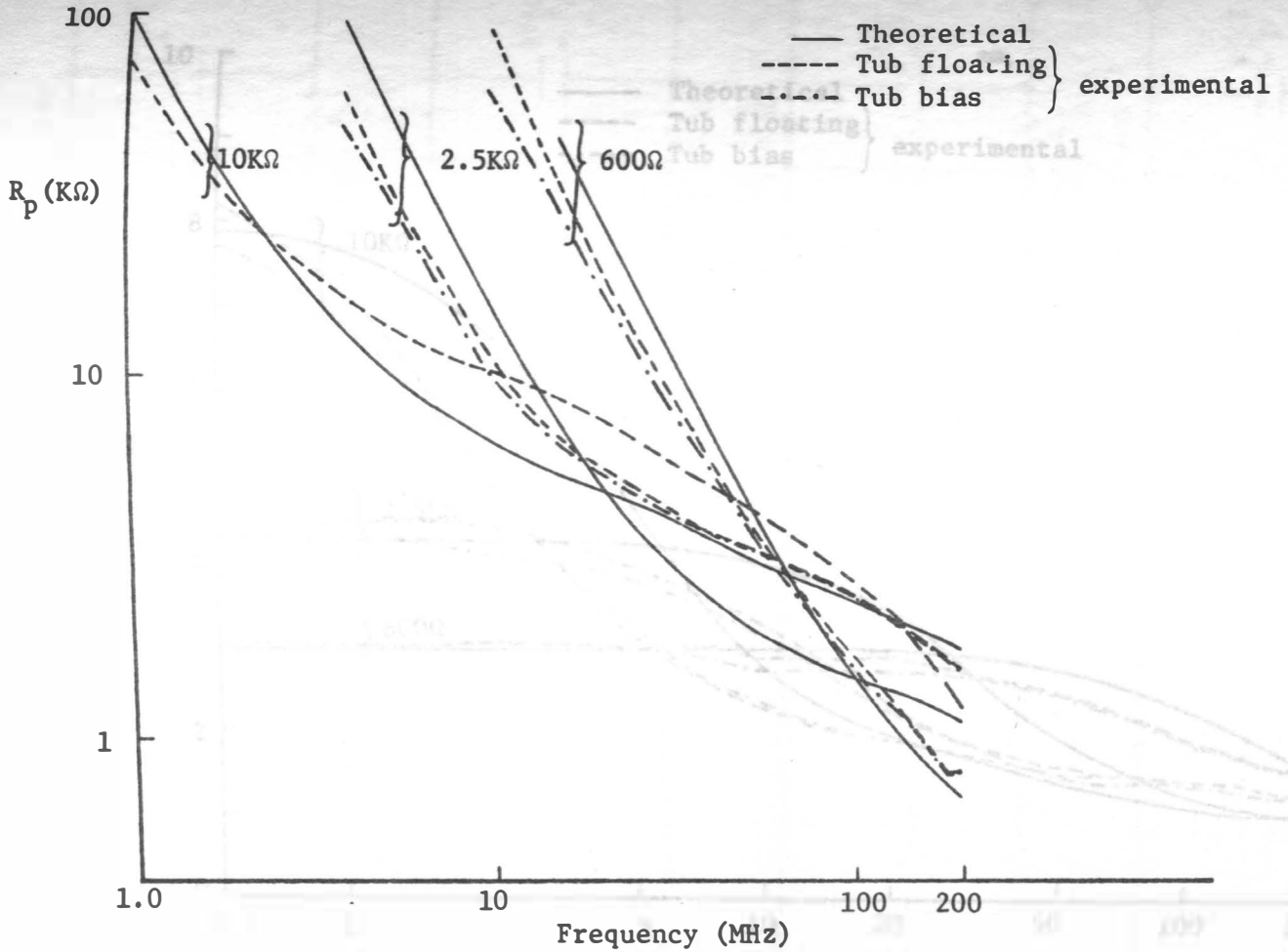



Fig. 4.40 Comparison between theoretical and observed equivalent parallel resistance--frequency responses for configuration-C.

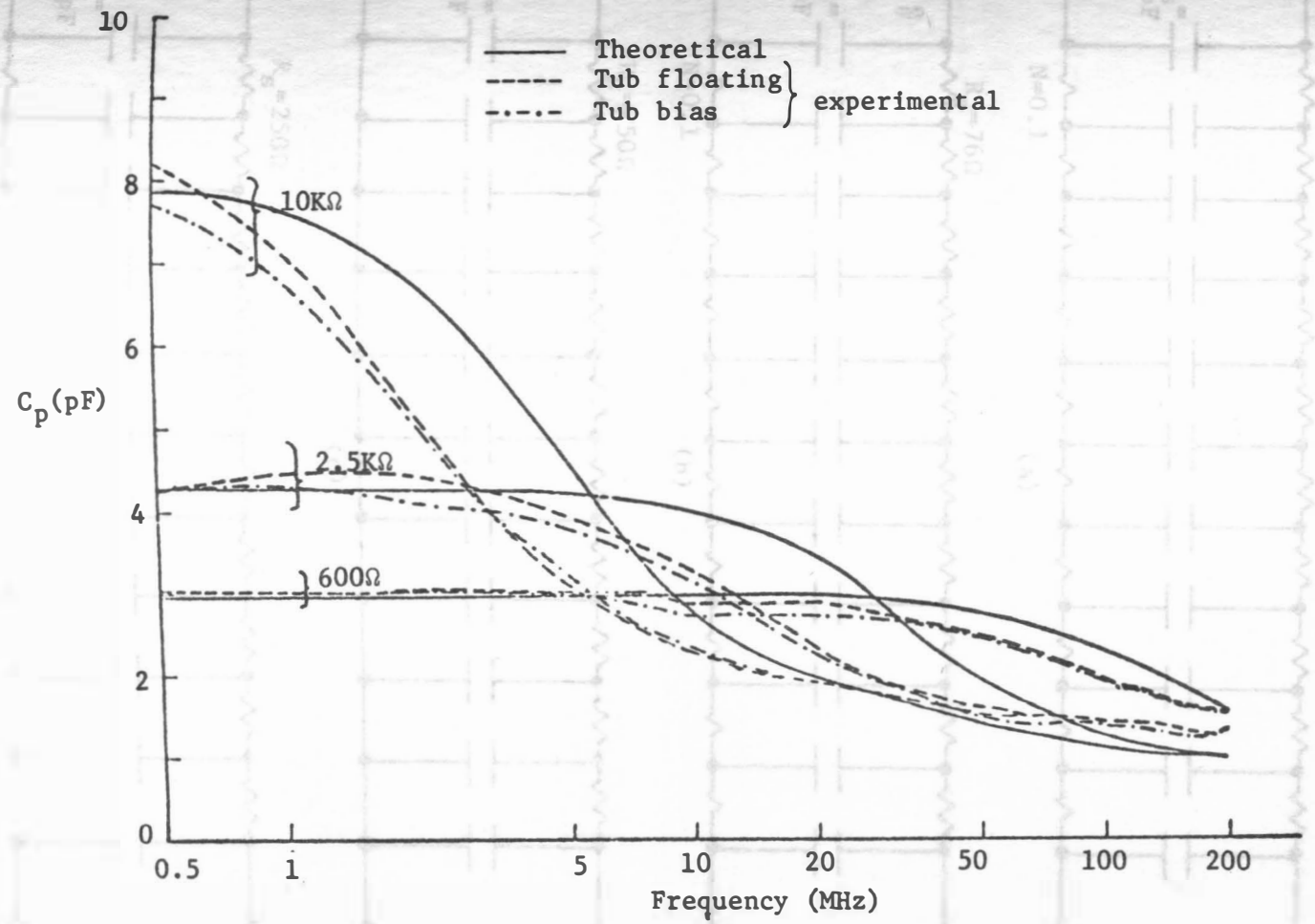
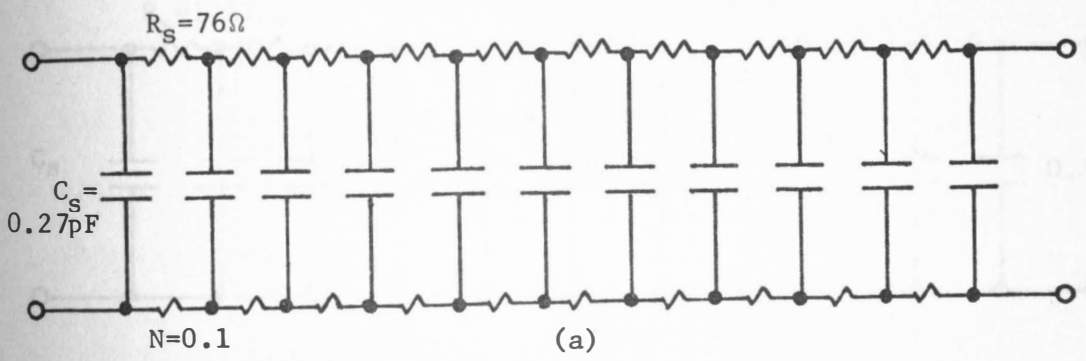
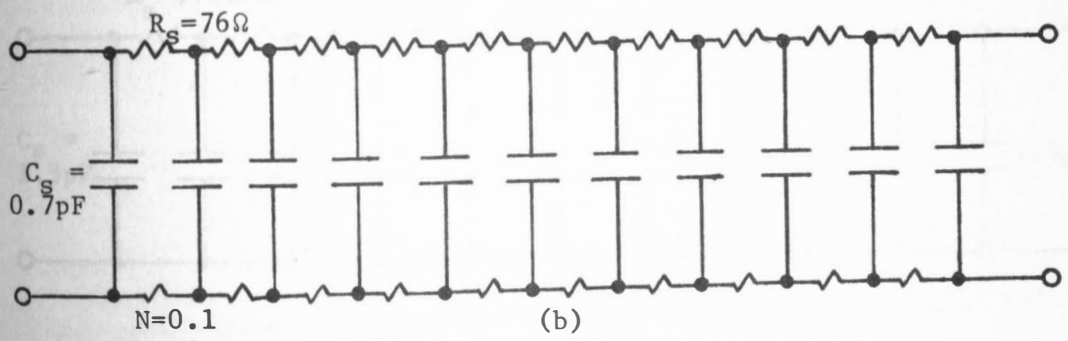


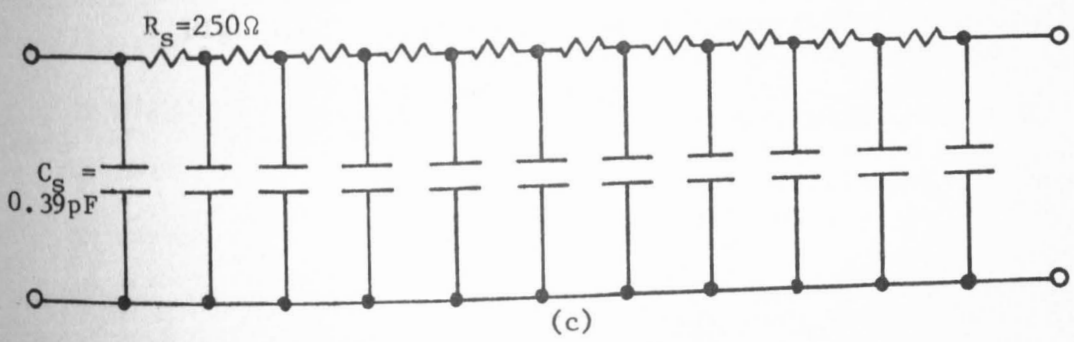

Fig. 4.41 Comparison between theoretical and observed equivalent parallel capacitance--frequency responses for configuration-C.


$R_s$=76Ω
$C_s$=
0.27pF
N=0.1

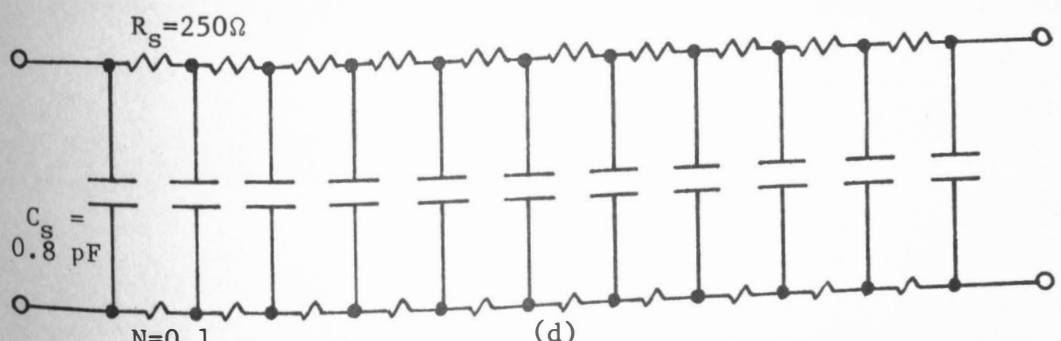
(a)


$R_s$=76Ω
$C_s$ =
0.7pF
N=0.1

(b)


$R_s$=250Ω
$C_s$ =
0.39pF

(c)


$R_s$=250Ω
$C_s$ =
0.8 pF
N=0.1

(d)

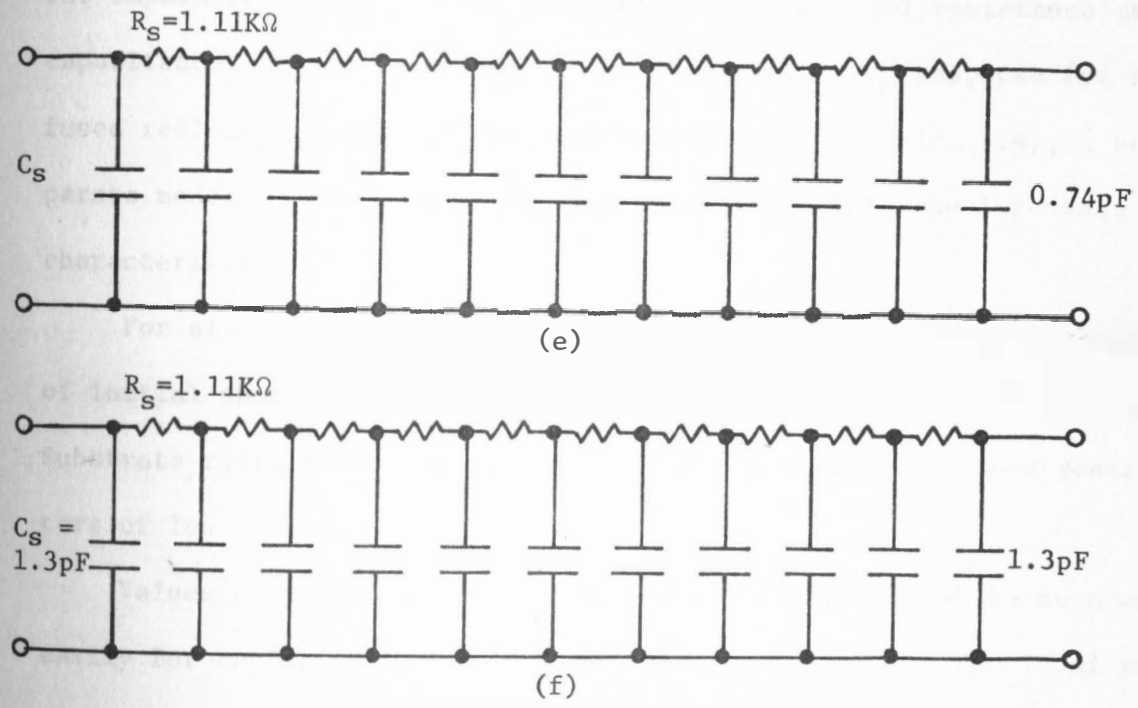



Fig. 4.42 Final models for diffused resistors
(a) 600Ω resistor configurations-A & C,
(b) 600Ω resistor, configuration-B,
(c) 2.15KΩ resistor, configurations-A & C,
(d) 2.15KΩ resistor, configuration-B,
(e) 10KΩ resistor, configurations-A & C, and
(f) 10KΩ resistor, configuration-B.

the impedance characteristics and equivalent parallel resistance and capacitance, $R_p$ and $C_p$, close to the actual observed response for diffused resistors. However, for configuration-B (see Fig. 3.4), a separate model is required which also closely predicts the impedance characteristics.

For all these configurations a ten segment distributed RC network of initial shunt capacitance type provides a good model (see Fig. 4.8(b)). Substrate resistance could be included for models of diffused resistors of low values.

Values of sectional capacitances and resistances can be determined easily for configurations-A and -C. The values for the sectional resistance is one-tenth of the total low-frequency value of resistance measured for the diffused resistor. For the sectional value of the capacitance, measurement of equivalent parallel capacitance with output port open is required. Since there are eleven capacitances for a ten segment initial shunt capacitance network, section capacitance $C_s$ is one-eleventh of the equivalent parallel capacitance $C_p$. Thus the expressions for sectional resistance and capacitance values for configurations-A and -C could be written as

$$R_{sectional} = \frac{\text{Value of diffused resistor at low frequency}}{10}$$

$$C_{sectional} = \frac{\text{Value of equivalent parallel capacitance with output open}}{11}$$

Another method of determining $C_s$ could be by measuring the equivalent parallel capacitance $C_p$ at low frequencies by connecting diffused re-

sistor in configuration-A and then using Eqn. (4.22).

A theoretical model for a diffused resistor in configuration-B could also be obtained by using a 10 segment distributed RC network with initial shunt capacitance. This network may include substrate resistance if a model for low values of diffused resistors is desired. Value of N selected could be nearly 0.1.

The value of sectional resistance is equal for this configuration and for configuration-A or -C. The sectional value of capacitance is obtained by measuring the equivalent parallel capacitance $C_p$ at low frequencies, connecting the diffused resistor in configuration-B. This provides a satisfactory model for impedance characteristics for a diffused resistor in configuration-B.

# CHAPTER V

# DIODES AND TRANSISTORS

This chapter presents the results of studies made on monolithic diodes and transistors. The objective of the diode study is to find a small signal a-c model to explain the measured capacitance and resistance values of different configurations. The forward bias characteristics and d-c current gain of different p-n junctions in transistors is reported in this chapter.

## 5.1 Monolithic Diodes

Diodes find widespread use in integrated circuits used in digital applications. This is particularly evident from the large number of diodes utilized in DTL circuits. Of course, diodes are used in integrated circuits in many other applications. A monolithic diode may be fabricated by making a single p-type base diffusion into the n-type layer. Alternately a diode may be obtained by connecting together the various regions of a transistor. It is a common practice to use transistors in this way because transistors can be obtained more readily than specialized diode structures.

Fig. 5.1 shows the five different ways in which the monolithic transistor structure can be utilized as a diode and presents each connection arrangment schematically as well as structurally.

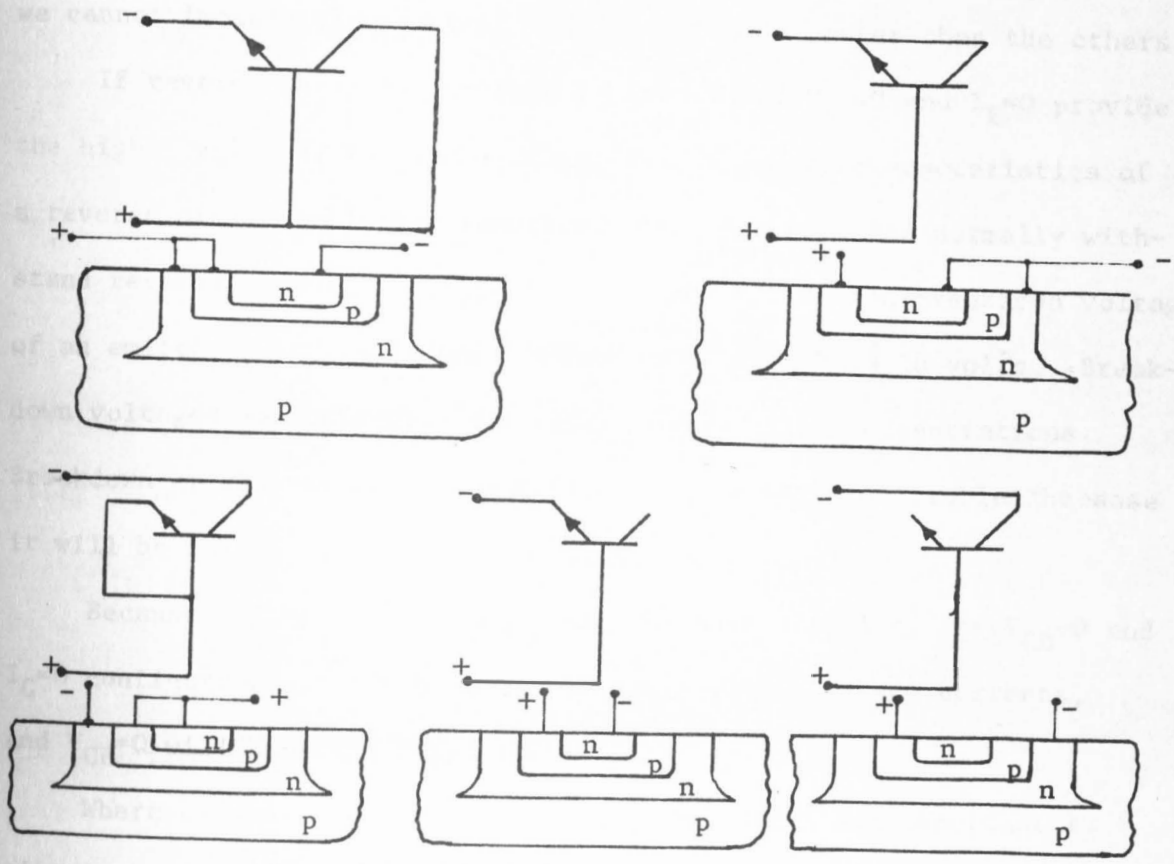



Fig. 5.1 IC diode connections

These five possible diode configurations are:

(a) Emitter-base junction--collector shorted to base ($V_{CB}$=0)

(b) Collector-base and emitter-base junction connected in parallel ($V_{CE}$=0)

(c) Collector-base junction--emitter shorted to base ($V_{EB}$=0)

(d) Emitter-base junction--collector floating ($I_C$=0)

(e) Collector-base junction--emitter floating ($I_E$=0)

In order to conveniently discuss these five cases we will use the equations in parenthesis as names for connections. The five methods of diode fabrication actually result in different characteristics, and

we cannot immediately say that one is obviously better than the others.

If reverse breakdown voltage is important, $V_{EB}=0$ and $I_E=0$ provide the higher voltage, for these connections have the characteristics of a reverse biased collector junction. That junction can normally withstand reverse potentials of 30 volts or more while the breakdown voltage of an emitter junction is more likely to be from 5 to 10 volts. Breakdown voltages are primarily determined by impurity concentrations. Breakdown of the collector-substrate diode presents no problem because it will be in the vicinity of 70 volts.

Because of the small area of emitter-base junction, the $V_{CB}=0$ and $I_C=0$ configurations will have the lowest reverse leakage currents, and $V_{CE}=0$ will have the largest.

Where capacitances associated with the diodes are important to circuit behavior $I_C=0$ yields about one-half of the largest capacitance. The worst case occurs for $V_{CE}=0$.

In digital applications, diode recovery time is indicative of the amount of stored charge that must be dissipated before a change in state from ON to OFF can be accomplished. The $V_{CB}=0$ connection has the largest recovery time because both junctions are simultaneously forward biased and this results in the largest amount of stored charge.

The lowest forward voltage drop at a given level of forward current is observed in diodes with $V_{CB}=0$. All other connections have about the same drop, 10% higher than the best performance.

### 5.1.1 Diode Capacitances

Fig. 5.2 shows the effective capacitances of the five diode configurations. $C_D$ denotes the diode capacitance and $C_P$ is the parasitic capacitance.

$C_{TS}$ is the capacitance of collector-substrate junction, $C_{TE}$ is the capacitance of emitter-base junction and $C_{TC}$ is the capacitance of collector-base junction. Here the collector-substrate or isolation junction contributes the third capacitance that has been considered.

In calculating the effective capacitance of each of the five diode configurations, we must consider both the capacitance across the diode and the capacitance of the collector-substrate junction $C_{TS}$. Since the substrate is normally connected to the most negative potential (for a p-substrate), the substrate terminal of $C_{TS}$ is at signal ground. The resultant capacitance network becomes a three terminal structure, with the collector-substrate capacitance appearing as a parasitic element.

Note that $I_C=0$ in Fig. 5.2(d) has the smallest parasitic capacitance.

### 5.1.2 Active Parasitics

In a microcircuit system, the p-type substrate is tied to the most negative point in the circuit to ensure that the collector-substrate junction is reverse biased. Thus under certain conditions of circuit operation it is possible to obtain transistor action in the p-n-p device comprising the base, collector and substrate regions

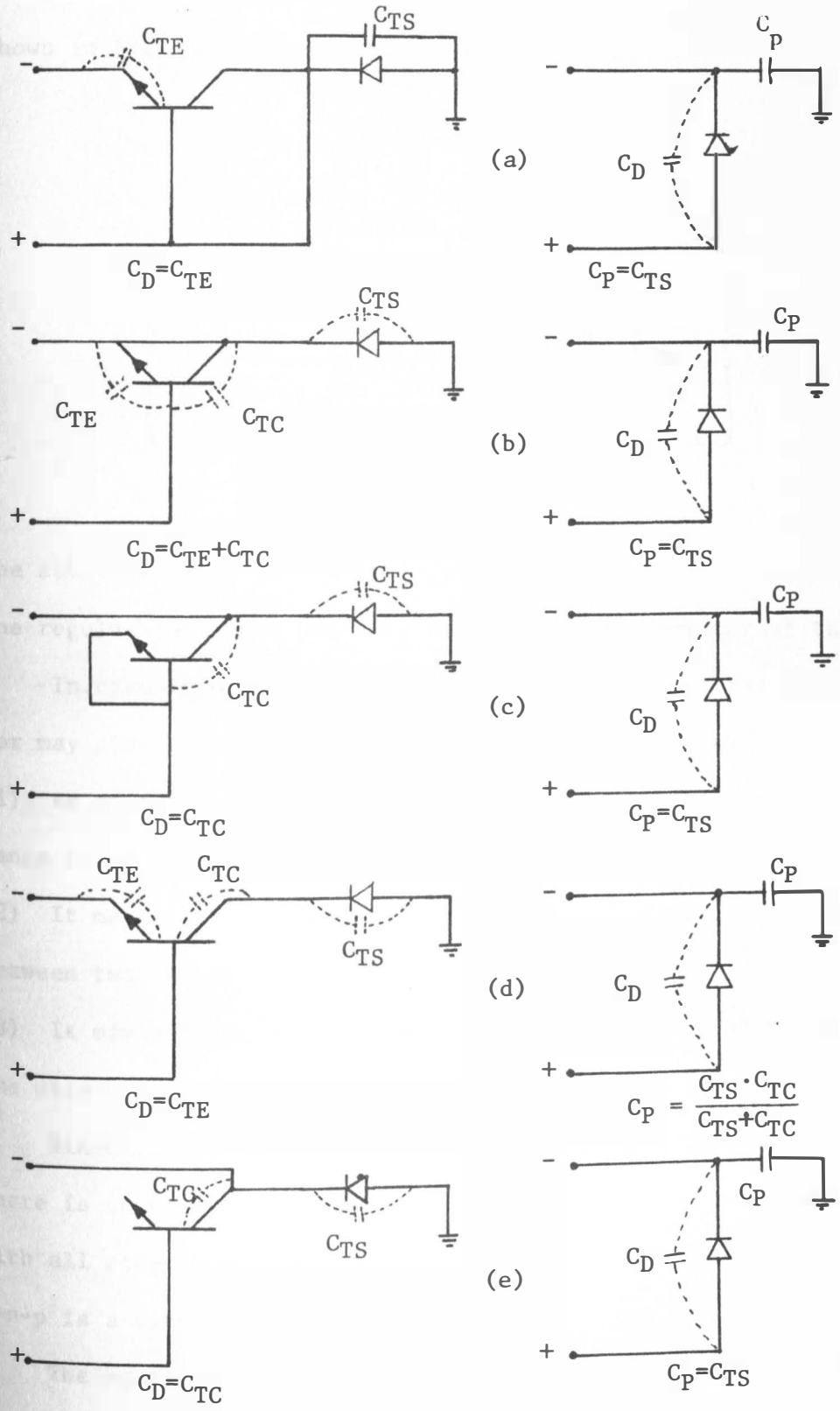



Fig. 5.2 Effective capacitances of five diode configurations.

shown in Fig. 5.3.

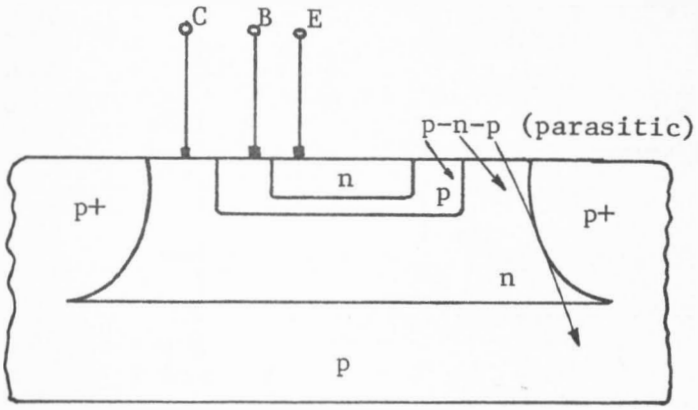



Fig. 5.3 Parasitic p-n-p transistor.

The substrate acts as the collector of the unwanted transistor, and the regular collector and base become base and emitter of the parasitic.

In circuit operation the presence of the p-n-p parasitic transistor may give rise to three different types of effects:

(1) As an active device it may introduce a variable parasitic impedance in the microcircuit of which it is a part.

(2) It may provide a "sneak" path by which unwanted coupling occurs between two otherwise isolated components.

(3) It may provide a shunt path which diverts part of the current in the circuit.

Since these regions are short-circuited in configuration $V_{CB}=0$, there is no possibility of active p-n-p effects in this configuration. With all other configurations the possibility of obtaining an active p-n-p is a very real one.

The equivalent circuits for these five diode configurations can be as shown in Fig. 5.4.

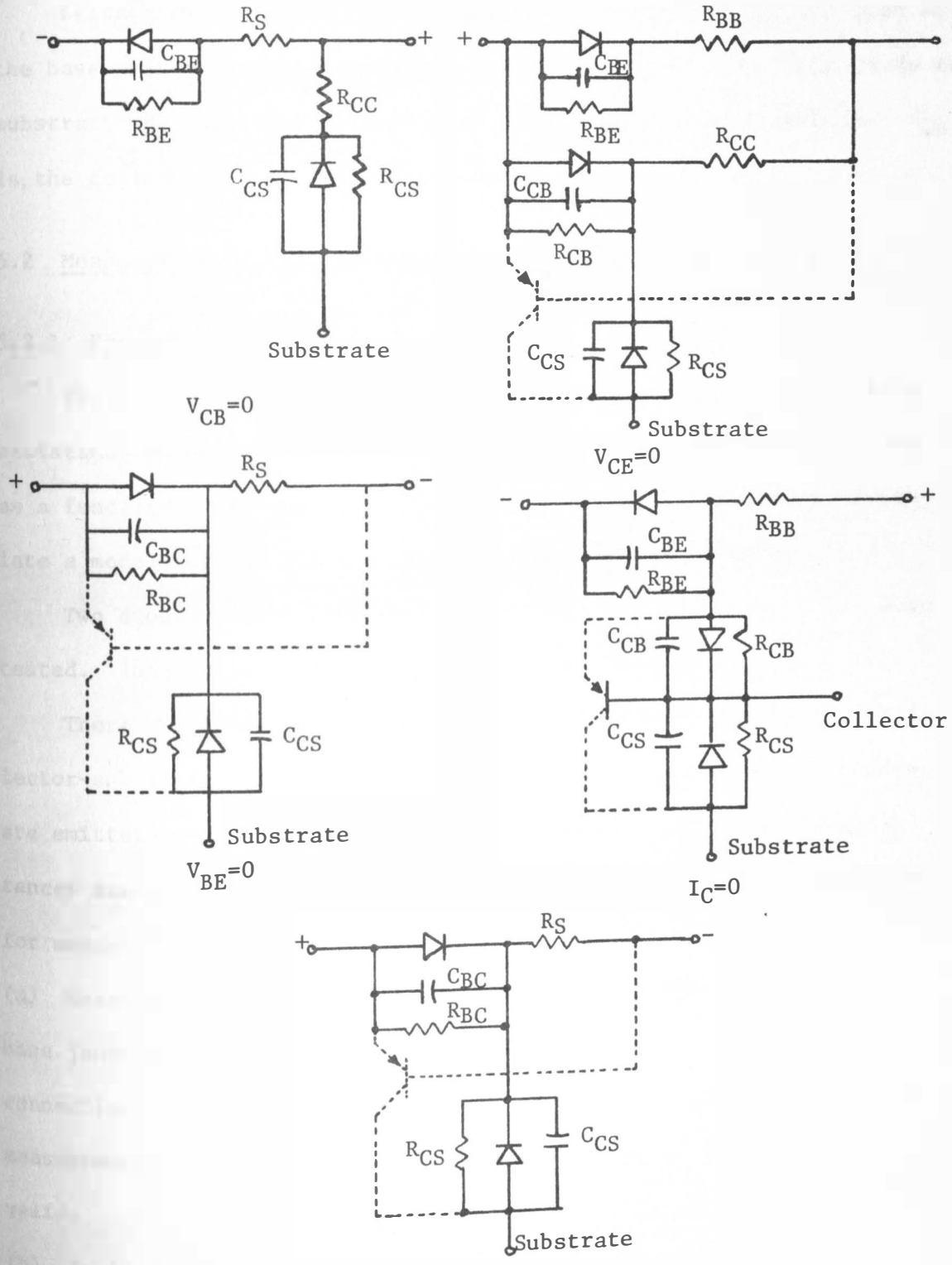



Fig. 5.4 Equivalent circuits for five diode configurations.

Leakage current path $R_{BE}$ and junction capacitance $C_{BE}$ are that of the base-emitter junction above; $C_{CS}$ is stray capacitance from anode to substrate; $R_{BB}$ is same as the series resistance of the transistor; $R_{CS}$ is the collector to substrate resistance.

## 5.2 Measurement of Parasitics Associated with Diodes

### 5.2.1 Experimental Setup

The aim is to measure the parasitic capacitance and the leakage resistance associated with the diode under reverse biased conditions as a function of frequency. Later, an attempt will be made to formulate a model for the diode to explain the observed behavior.

Two diodes, fabricated on Quickchip SG 3801 (see Fig. 5.5), were tested. These diodes are emitter-base junction diodes.

There are three junctions--emitter-base, base-collector and collector-substrate--associated with each transistor. Since the diodes are emitter-base junction diodes, to get an idea of various capacitances associated with these junctions the following setups were used for measurements.

(a) Measurement of resistance and capacitance between emitter and base junctions with substrate left floating. Fig. 5.6 describes this connection. As described in Fig. 5.4 for case of $I_C=0$ or $V_{CB}=0$ this measurement should lead to the estimation of $C_{BE}$ if that model is valid.

(b) To find the effect of substrate tied to the common end of the diode the connection shown in Fig. 5.7 is used.

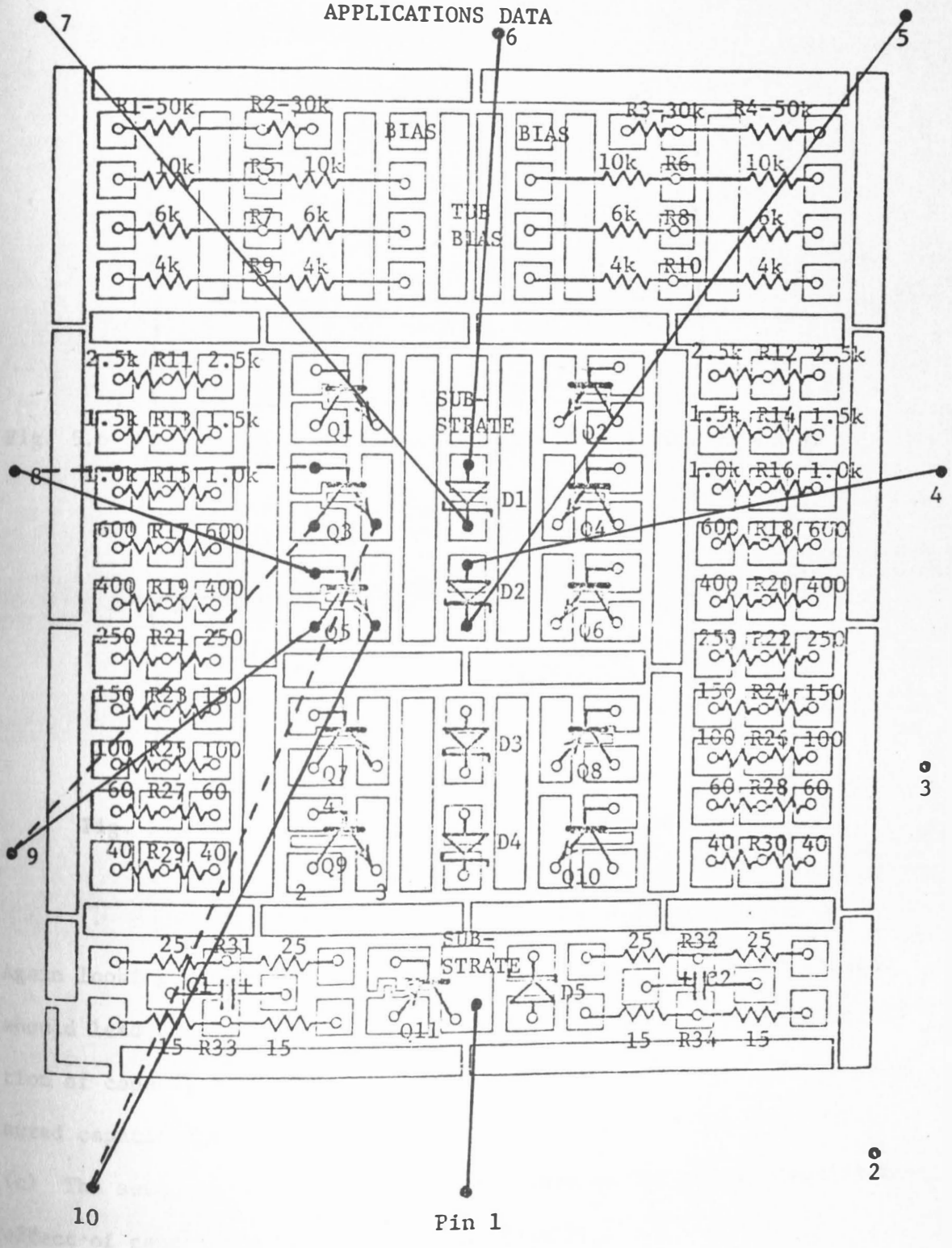



Fig. 5.5 Worksheet of Quickchip showing bonding connections.

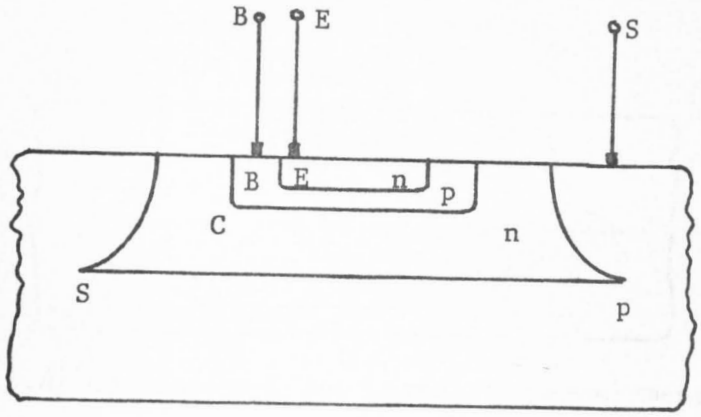



Fig. 5.6 Connection-A for parasitic capacitance measurements.

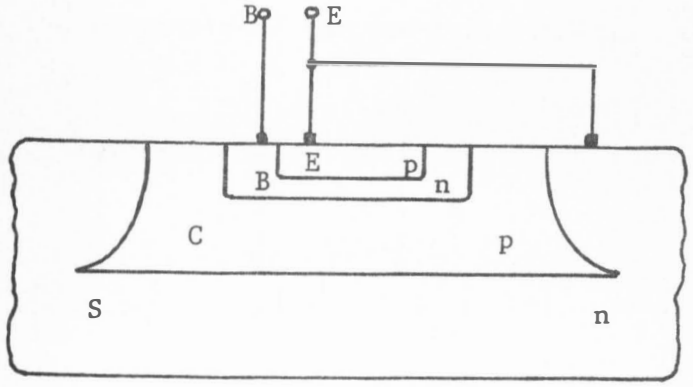



Fig. 5.7 Connection-B for parasitic measurements.

Again looking back to the case of $I_C$=0 in Fig. 5.4, this measurement should lead to the capacitance $C_{BE}$ in parallel with a series combination of capacitors $C_{CB}$ and $C_{CS}$. This should show an increment in measured capacitance value over connection-A.

(c) The setup shown in Fig. 5.8 should lead to the series capacitance effect of capacitors $C_{BE}$, $C_{CB}$ and $C_{CS}$ (see Fig. 5.4).

(d) In the Fig. 5.9 setup the positive end of the emitter-base junction diode was tied to the substrate effectively leaving capacitance

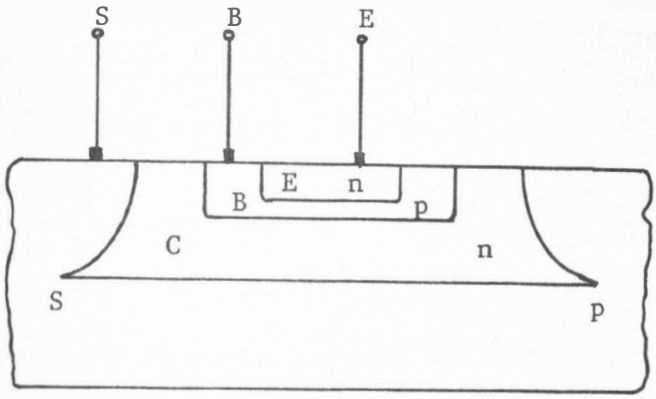



Fig. 5.8 Connection-C for parasitic measurements.

$C_{BE}$ between the terminals of the substrate and the cathode of the diode.

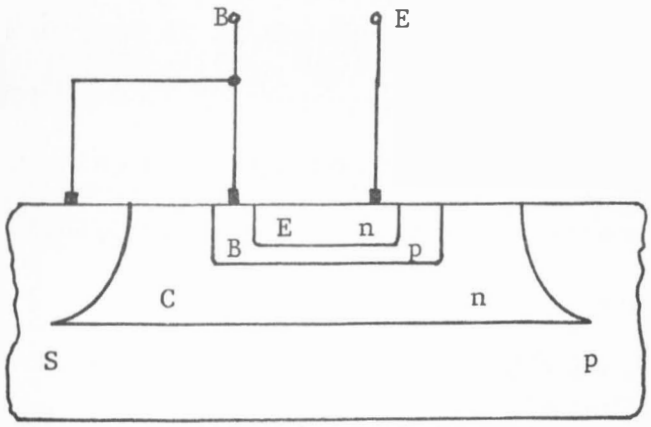



Fig. 5.9 Connection-D for parasitic capacitance measurements.

For all these connections, two cases were observed when practical: (a) no bias applied to the p-n junction; (b) with p-n junction reverse biased.

The $Y_{ie}$ board was used in all these measurements in conjunction with Boonton 250A RX Meter.

Pin connections for diodes 1 and 2 are indicated in Table 5.1 for all four connections described earlier (see Fig. 5.5).

| Connection | Diode 1 Pin Connected to | | | Diode 2 Pin Connected to | | |
|---|---|---|---|---|---|---|
| | E | B | C | E | B | C |
| A | 4 | 5 | - | 6 | 7 | - |
| | 5 | 4 | - | 7 | 6 | - |
| B | 5 | 4 | 1 | 7 | 6 | 1 |
| C | 1 | 5 | - | 1 | 7 | - |
| D | 4 | 5 | 1 | 6 | 7 | 1 |

Table 5.1 Pin connections of diodes for parasitic capacitance measurements.

### 5.2.2 Measurements

Tables I through IV in the Appendix describe the effective $R_p$ and $C_p$ measured for each of the four connections.

It can be noted that capacitance values remain fairly constant with changing frequency for all measured connections. However the value of resistance $R_p$ decreases to a low value starting from a very high value of nearly infinity. In various columns of Tables I through IV in the Appendix, $R_p$ has been indicated as infinity. Actually the RX Meter does not read values above 100 KΩ. So all the $R_p$ values much greater than 100 KΩ have been indicated as infinity in these tables.

The next section explains the cause for the decreasing nature of parallel resistance and nearly constant capacitance value, and an attempt is made to explain the observed capacitance values for different connections.

## 5.3 Equivalent Parallel Resistance and Capacitance of Diode

Table I in the Appendix indicates that the parallel capacitance $C_p$ stays constant with frequency but parallel resistance decreases to a low value at high frequencies. This might suggest that diode performance deteriorates at high frequencies because the leakage resistance seems to be decreasing at high frequencies. But from the analysis of a simple diode equivalent it can be seen that indeed it is a common phenomenon for any diode.

Let us consider a reverse-biased diode. Associated with it is a leakage resistance, which is of a large magnitude, and a junction capacitance which can be of the order of several pF for monolithic diodes. There is also a small series base spreading resistance $r_{bb'}$, as appears in hybrid-pi equivalent of a transistor. Thus a simple equivalent circuit is shown in Fig. 5.10.

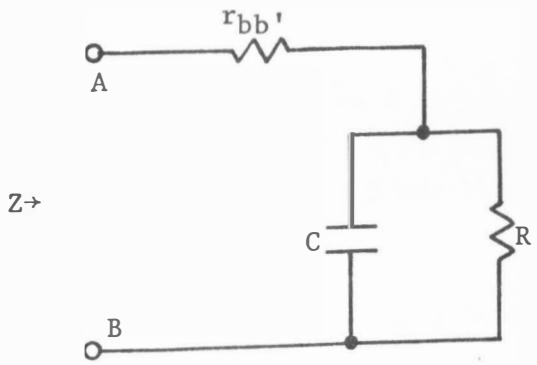



Fig. 5.10 Simple equivalent circuit of a diode.

Input impedance looking into terminals A and B is:

$$\text{Impedance } Z = r_{bb'} + \frac{R}{1+j\omega RC}$$

or

$$\text{Admittance } Y = \frac{1 + j\omega RC}{(r_{bb'} + R) + j\omega RCr_{bb'}}$$

Separating the real and imaginary parts of admittance

$$\text{Real } Y = \frac{(r_{bb'}+R) + \omega^2R^2C^2r_{bb'}}{(r_{bb'}+R)^2 + \omega^2R^2C^2r_{bb'}^2} \tag{5.1}$$

$$\text{Im } Y = \frac{j\omega R^2C}{(r_{bb'}+R)^2 + \omega^2R^2C^2r_{bb'}^2} \tag{5.2}$$

Equivalent $R_p$ looking into terminals A and B will be the inverse of Eqn. (5.1):

$$\text{Equivalent } R_p = \frac{1}{\text{Real } Y} = \frac{(r_{bb'}+R)^2 + \omega^2R^2C^2r_{bb'}^2}{r_{bb'} + R + \omega^2R^2C^2r_{bb'}} \tag{5.3}$$

Let $r_{bb'}+R = A$ and $R^2C^2r_{bb'} = B$

then

$$\text{Equivalent } R_p = \frac{A^2 + B\omega^2 r_{bb'}}{A + B\omega^2} \tag{5.4}$$

and

$$\text{Equivalent } C_p = \frac{R^2C}{A^2 + B\omega^2} \tag{5.5}$$

Here A and B are constants since R, C and $r_{bb'}$ have been assumed to be constant.

With the increase of frequency the term $B\omega^2$ keeps on increasing at a rapid rate. From Eqn. (5.4) it can be seen that since $A^2 >> A$ (A being the order of $10^6$), the term $B\omega^2$ will start having appreciable effect in the denominator much earlier than it will have on the numerator with increasing frequency. So, the numerator does not change appreciably while the denominator increases, hence decreasing equivalent $R_p$ with

increasing frequency. At high frequencies of the order of 200 MHz the term $B\omega^2 r_{bb'}$ starts having effect on the numerator. The denominator still increases at a rapid rate compared to the numerator, effectively decreasing $R_p$. This expression leads to an asymptotic value of $r_{bb'}$ at extremely high frequencies.

Table 5.2 lists the equivalent $R_p$, numerator, denominator, A, $A^2$ and $B\omega^2$ values for Eqn. (5.4). Values of $r_{bb'}$, R and C have been arbitrarily chosen.

Let $r_{bb'} = 40\Omega$ $R = 10^6\Omega$ $C = 5.0$ pF

| Frequency (MHz) | A | $A^2$ | $B\omega^2$ | Numerator | Denominator | $R_p$ |
|---|---|---|---|---|---|---|
| 1 | $\sim 10^6$ | $\sim 10^{12}$ | $\sim 16\times10^5$ | $\sim 10^{12}$ | $104\times10^4$ | $\sim 1M\Omega$ |
| 10 | $\sim 10^6$ | $\sim 10^{12}$ | $\sim 16\times10^7$ | $\sim 10^{12}$ | $5\times10^6$ | $0.2M\Omega$ |
| 50 | $\sim 10^6$ | $\sim 10^{12}$ | $\sim 4\times10^9$ | $\sim 10^{12}$ | $101\times10^6$ | $\sim 10K\Omega$ |
| 100 | $\sim 10^6$ | $\sim 10^{12}$ | $\sim 16\times10^9$ | $\sim 10^{12}$ | $\sim 4\times10^8$ | $\sim 2.5K\Omega$ |
| 200 | $\sim 10^6$ | $\sim 10^{12}$ | $\sim 64\times10^9$ | $\sim 1.06\times10^{12}$ | $\sim 16\times10^8$ | $\sim 625\Omega$ |

Table 5.2 Various calculated values for Eqn. (5.4).

Now let us consider Eqn. (5.5). It can be seen that the denominator is the same as the numerator of Eqn. (5.4). As already noted (see Table 5.2) the numerator of Eqn. (5.4), or the denominator of Eqn. (5.5), does not change appreciably. Because the $R^2C$ term (numerator of Eqn. (5.5)) is constant, we could say that whole expression for $C_p$ remains almost constant. To some approximation:

$$\text{Equivalent } C_p \simeq \frac{R^2C}{(r_{bb'}+R)^2} \simeq \frac{R^2C}{R^2} = C \qquad (5.6)$$

This explains why capacitance $C_p$ stays almost constant with increasing frequency. Actually at very high frequencies there should be a decrease in the capacitance value.

## 5.4 Capacitance Variation for Four Connections

Now we explain the nature of variation of capacitance from one connection to another, based upon the equivalent circuit of the monolithic diode.

Let us consider the $I_C$=0 case in Fig. 5.4. For simplicity we consider only the various capacitances and ignore the leakage resistances. Such a model is shown in Fig. 5.11.

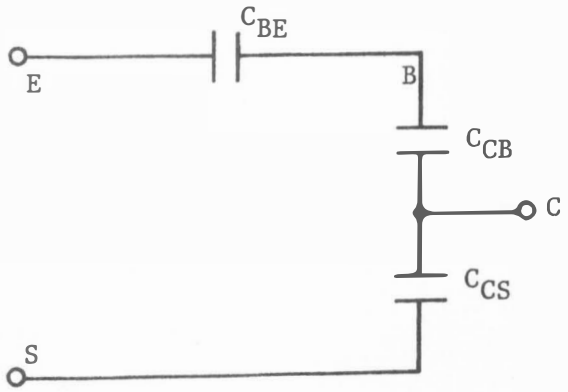
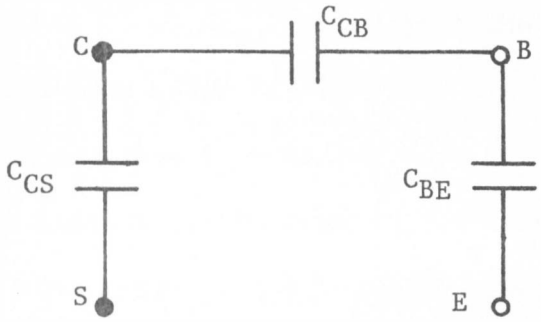



Fig. 5.11 Capacitance model for a monolithic diode.

Fig. 5.12 lists the effective connections for connections-A through D and equivalent capacitance $C_p$. From analysis of these expressions for effective parallel capacitance $C_p$, we can expect more capacitance $C_p$ for connection-B than for connection-A.

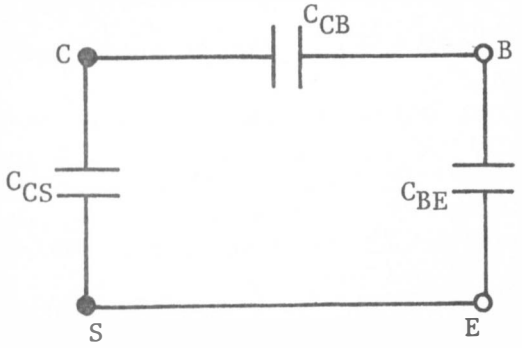
In connection-C capacitances $C_X$ and $C_{BE}$ appear in series. Because they are both of the same order of magnitude, the expected $C_p$ should

Connection-A



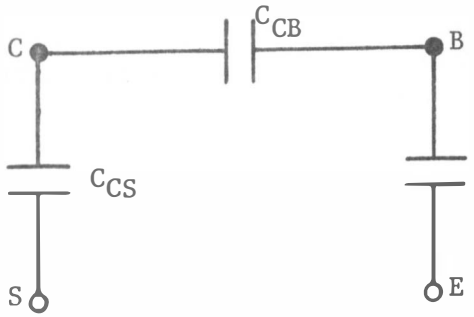

$$C_p = C_{BE}$$

Connection-B




$$C_p = C_{BE} + \frac{C_{CS} \cdot C_{CB}}{C_{CS}+C_{CB}}$$

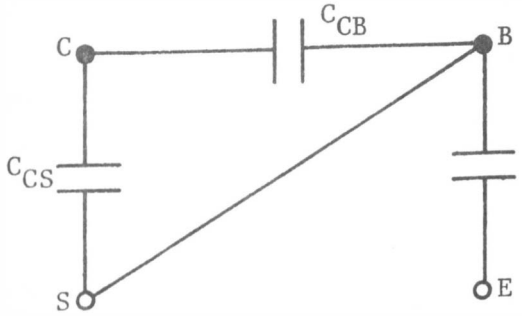
Connection-C




$$C_p = \frac{C_{BE} \cdot C_X}{C_{BE}+C_X}$$

$$C_X = \frac{C_{CS} \cdot C_{BE}}{C_{CS}+C_{BE}}$$

Connection-D




$$C_p = C_{BE}$$

Fig. 5.12 Effective capacitance seen for various connections.

be less than either $C_X$ or $C_{BE}$, and smaller than the smaller of $C_X$ and $C_{BE}$. But as seen from Table III in the Appendix, for connection-C the values of capacitance $C_p$ observed are more or less equal to the values given in Table I in the Appendix for connection-A. Perhaps this indicates that this model is not sufficient to explain the observed behavior of connection-C.

For connection-D one should expect to see $C_{BE}$ and hence the observed $C_p$ is expected to be close in value to that of Table I in the Appendix for connection-A. But comparing the values in Table I (connection-A) and Table IV in the Appendix (connection-D) a difference is seen to exist. Values of Table IV seem to be slightly less than those of Table I in the Appendix. Though a difference does exist, it is difficult to say how significant this difference is. On the RX Meter, the least count is 0.1 pF.

It can be concluded that the model of Fig. 5.4 is not sufficient to explain the observed behavior. This model should be modified (maybe by some extraneous capacitance) to take care of behavior in connection-B.

Since in connection-B, capacitance values are larger than others, it does not seem possible to explain this unless an extra capacitance is added between emitter and substrate. As a trial, capacitance model shown in Fig. 5.13 was considered. Here $C_1$ is the emitter-base junction capacitance. Base-collector and collector-substrate capacitances have been combined and represented as one capacitance $C_2$. $C_3$ is the new capacitance added. Fig. 5.14 shows the different connections and

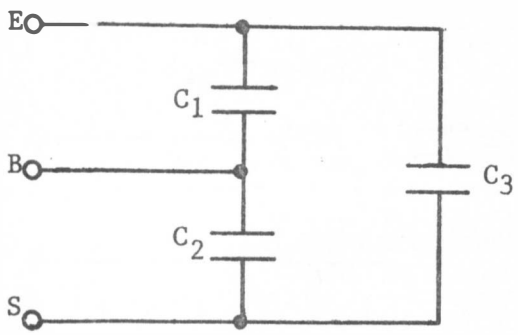
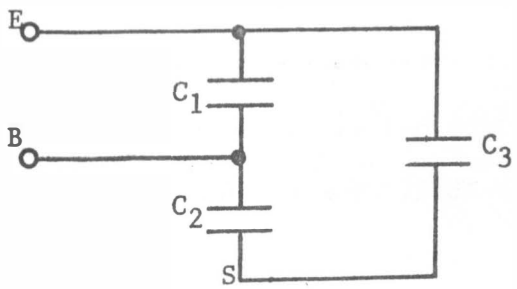



Fig. 5.13 Modified capacitance model for a monolithic diode.

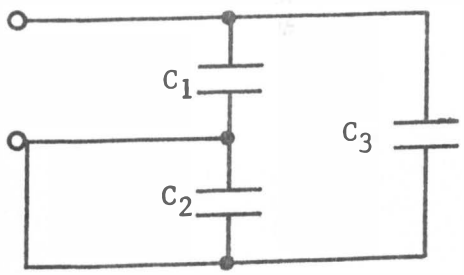
values of $C_p$ expected for all four connections.

Connection-A



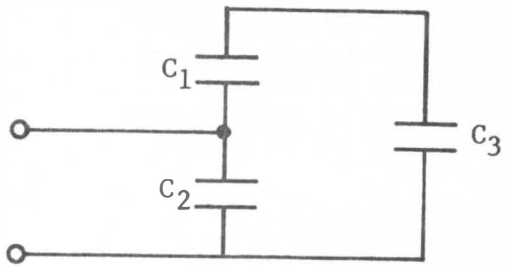

$$C_p = C_1 + \frac{C_2 \cdot C_3}{C_2 + C_3}$$

Connection-B



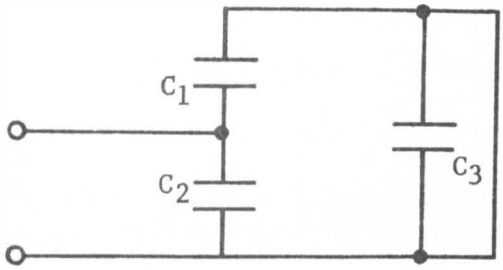

$$C_p = C_1 + C_3$$

Connection-C




$$C_p = C_2 + \frac{C_1 \cdot C_3}{C_1 + C_3}$$

Connection-D




$$C_p = C_1 + C_2$$

Fig. 5.14 Effective capacitance seen for modified capacitance model.

We will try to solve these equations for the unknown capacitances $C_1$, $C_2$ and $C_3$. There are three unknowns but four equations. If a solution does exist then one equation is redundant. Taking the first three equations and 1.85 pF, 2.85 pF and 1.8 pF to be the average values of $C_p$ observed for these cases respectively, we have:

$$C_1 + \frac{C_2 \cdot C_3}{C_2 + C_3} = 1.85$$

$$C_1 + C_3 = 2.85$$

$$C_2 + \frac{C_1 \cdot C_3}{C_1 + C_3} = 1.8$$

Approximate solution to these equations is:

$$C_1 = 1.18 \text{ pF}$$

$$C_2 = 1.11 \text{ pF}$$

$$C_3 = 1.67 \text{ pF}$$

If these values are used for connection-D we get

$$C_p = C_1 + C_2 = 2.29 \text{ pF}$$

The observed value of $C_p$ for connection-D is however only 1.65 pF. Hence this set of values is not conformable to the actual diode. If a solution of some other three equations instead of the first three is attempted, in some cases no real solution exists. We can conclude that no solution satisfying all four equations exists. Hence, not even this model is adequate to explain the trend of capacitance values for all four connections.

It was thought that perhaps the distributed nature of parasitic capacitance might explain the situation. So it was decided to propose a model as shown in Fig. 5.15. The values of capacitances were as calculated earlier.

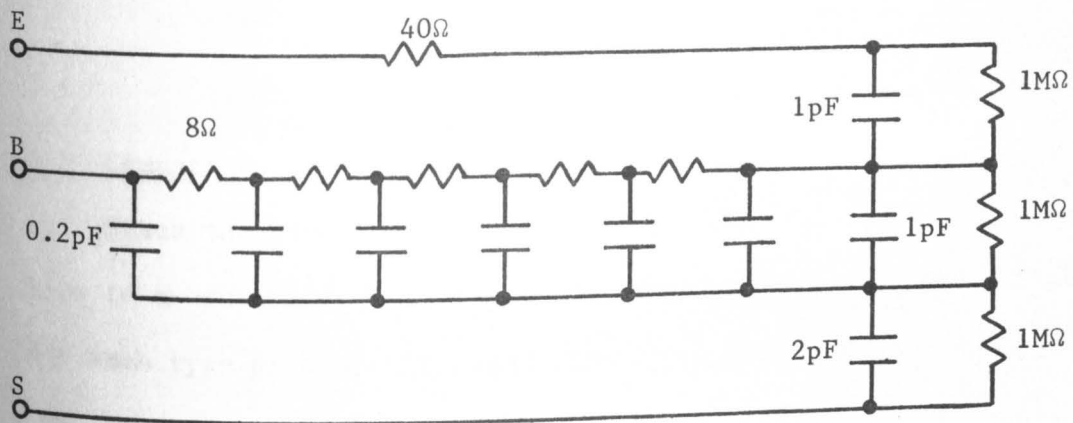



Fig. 5.15 Hypothetical distributed model for monolithic diode.

Even this did not seem to help. The observed trend in the four cases is distinctively different from that observed in more than one case. Certainly this does not represent the actual diode.

We can conclude that model of Fig. 5.13 cannot be accepted as a model for monolithic diode. This model fails to explain the observed behavior in all the four cases. Perhaps due to the effect of some extraneous capacitance or some other effect not considered so far, this model falls short of expected behavior. Complete model of Fig. 5.13 with leakage resistance is depicted in Fig. 5.16.

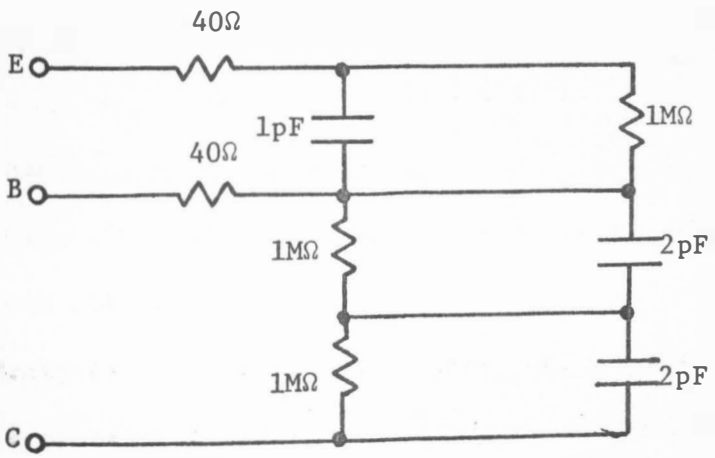



Fig. 5.16 A model for monolithic diode.

## 5.5 Comparison with Transistor Diode

Since the nature of the variation of capacitances from one connection to another does not seem to be explainable by the simple model for such type of diode, a transistor built on the same chip was studied to compare the two. Since diodes are emitter-base junction

diodes, a similar type of diode can be obtained by using the emitter-base junction of a transistor made on the chip. It was decided to measure the capacitance of such a diode in all the four connections and then compare the nature of variation to the measured values for diodes on the chip (Tables I through IV in the Appendix).

Transistor $Q_3$ was used. Pin connections initially made for $Q_5$ were removed and connected to $Q_3$ (dotted Connection in Fig. 5.5).

Table V through VIII in the Appendix give the measured values of capacitances and resistances for emitter-base junction of $Q_3$ transistor with collector left floating. No bias was applied for all these cases. Again the RX Meter in conjunction with the $Y_{ie}$ board, as described earlier, was used.

Tables IX through XII in the Appendix present the same set of measurements but with collector shorted to base and emitter-base junction used as the diode.

Comparing Tables V through VIII to Tables I through IV in the Appendix in a sequential order, i.e. I and V, II and VI, etc., we find that comparison is not good. In Tables I through IV in the Appendix, the values for connection-B are higher than rest of the connections. But for connections-A, C and D values are almost the same except that for connection-D they seem to be a little less than for connections-A and -C. While in Tables V through VIII in the Appendix values for connections-B, -C and -D seem to be quite comparable and equal in value while values for connection-A are considerably lower comparitively. Thus no favorable comparison is apparently visible.

Tables IX through XII in the Appendix seem to compare rather favorably with Tables I through IV in the Appendix respectively. In Tables IX through XII for connections-A, C and D in some cases values are almost the same as is true for connections-A, C and D in Tables I through IV in the Appendix. Higher values for connection-B (Table X in the Appendix) also compare with higher values in Table II in the Appendix for the same connection. Thus, the nature of variation seems to be the same except that in Table X values seem to be almost double those of the other connections. Differences are not so great for values in Table II compared to Tables I, III and IV in the Appendix.

So capacitance variation trend in case of monolithic diodes on the chip compares favorably well with diodes connected up from the transistors (base shorted to collector, emitter base junction used as diode). From this, perhaps it can be concluded that the same effect seems to be playing part for observed capacitance variation in both the cases. This presents a contradiction because the data sheet of Quick Chip SG 3801 mentions the diodes as E-B junction diodes. The chip under a microscope does not show any connection suggesting that the collector is shorted to base. So perhaps the diodes are E-B junction diodes with $I_C=0$. In that case diodes connected from transistors do not have same trend of variation as these actual diodes. This suggests that there is perhaps some other effect not considered so far that is causing the variation of capacitance from expected values.

Attention was shifted to d-c characteristics of different transistor junctions, as presented in the following section.

## 5.6 D-C Characteristics of Transistors

### 5.6.1 Characteristics of Different p-n Junctions in Transistors

There are four types of transistors available on the chip: high frequency n-p-n, medium current n-p-n, lateral p-n-p and common collector p-n-p. Since almost all these type of transistors differ from each other in physical dimensions, perhaps some variations in d-c characteristics can also be expected. Keeping this in mind, a study was made with the aim of finding the differences, if any, among the junctions in all four types of transistors. With the exception of the common collector p-n-p transistor, the transistors have three available p-n junctions: emitter-base, base-collector and collector-substrate. Only two junctions, emitter-base and base-collector, are available for the common collector p-n-p device.

Forward bias and reverse bias characteristics of these junctions were obtained experimentally. The simple circuit shown in Fig. 5.17 was used to obtain the junction characteristics.

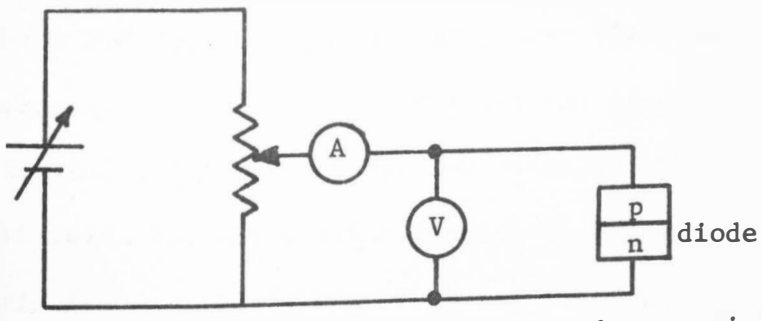



Fig. 5.17 Circuit for measuring forward bias characteristics of p-n junctions.

Fig. 5.18 shows the junction forward characteristics plotted for all four types of transistors.

Table 5.3 gives the reverse breakdown voltage estimated for these four types of transistor junctions.

| | Lateral PNP | | | Medium Current NPN | | | High Frequency NPN | | | Common Collector PNP | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Junction | E-B | B-C | B-S | E-B | B-C | C-S | E-B | B-C | C-S | E-B | B-C |
| Break-down Voltage | >72 | ∿6.4 | >72 | ∿6.0 | >30 | - | 5.8 | - | - | ∿6.0 | >30 |

Table 5.3 Approximate breakdown voltages of different p-n junctions in the transistors.

5.6.2 Analysis

From the V-I characteristics apparently little difference exists between the p-n junction characteristics of four different types of transistors: Lateral p-n-p, high frequency n-p-n, medium current n-p-n and common collector p-n-p. Only a slight shift is noted for collector-substrate (C-S) junction over base-collector (B-C) and for base-collector (B-C) junction over emitter-base (E-B) junction. This suggests that a slightly less forward breakdown voltage is expected for C-S junction (or B-S junction in lateral p-n-p) than for B-C junction of the same transistor. Similarly, a slightly smaller breakdown voltage is expected for B-C junction than for E-B junction. Here the purpose is to explain, if possible, the shift between E-B, B-C and C-S junction V-I characteristics as seen in Fig. 5.18 and the actual nature of variation of I with V.

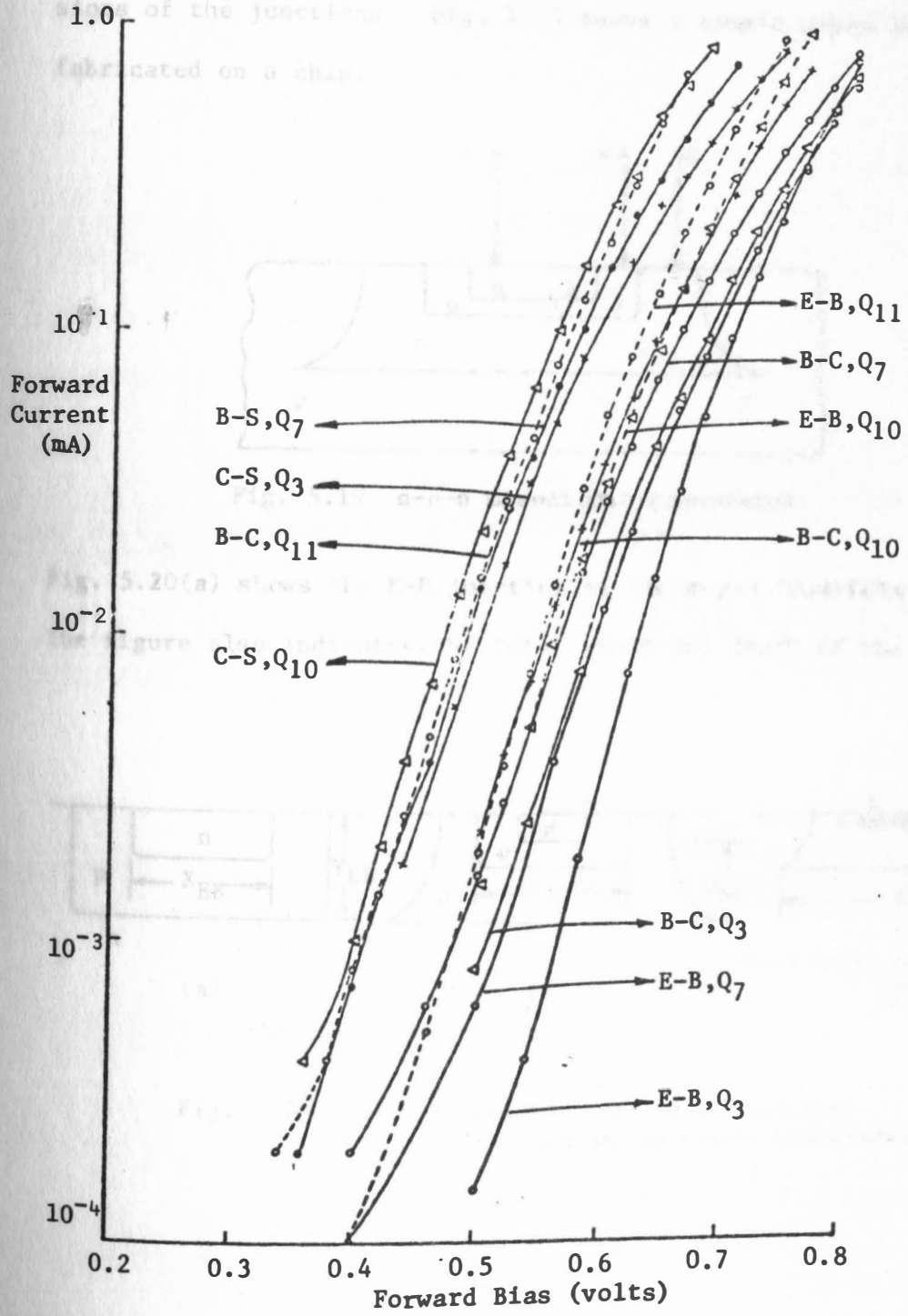



Fig. 5.18 Forward bias characteristics of all three p-n junctions in all transistor types.

Perhaps the phenomenon of the shift of junction characteristics of E-B, B-C and C-S junctions can be explained by the physical dimensions of the junctions. Fig. 5.19 shows a simple n-p-n transistor fabricated on a chip.

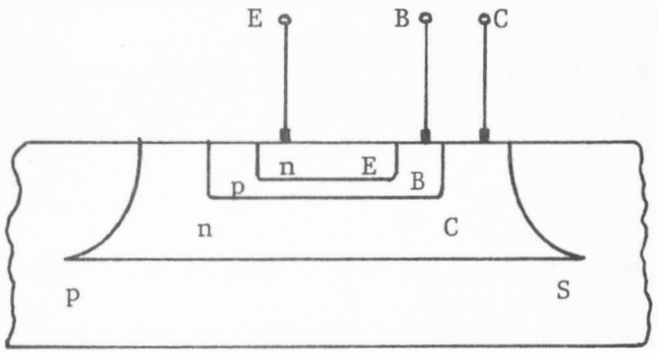



Fig. 5.19 n-p-n monolithic transistor.

Fig. 5.20(a) shows the E-B junction of the n-p-n transistor separately. The figure also indicates the total width and depth of the junction

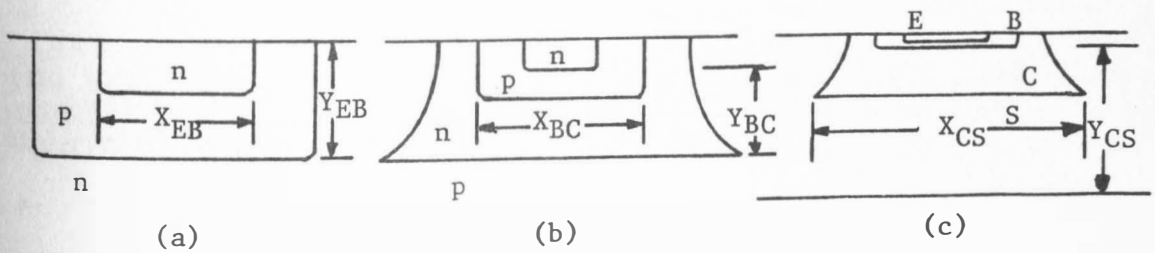



Fig. 5.20 (a) E-B junction (b) B-C junction
(c) C-S junction of an n-p-n transistor.

$X_{EB}$ denotes the width of the E-B junction and $Y_{EB}$ denotes the depth of this junction. Subscripts denote the junction in consideration. Figs. 5.20 (b) and 5.20 (c) denote the same things for B-C and C-S junctions. It can be seen from the figures that both X and Y progressively increase from E-B to B-C and B-C to C-S junctions. Since junction area is important, to get a complete picture of the effective area of the p-n junction it is also necessary to consider the other dimension involved with X in the area. Fig. 5.21 shows the top view of monolithic n-p-n transistor. It can be seen that length Z multiplies X to give the effective area to be considered for the junction. It should be kept in mind that this gives a rough estimate of the area. Since the contacts for emitter or base or any other area are not made on the two opposite ends of the bar, as would be the case in a simple diode structure, current does not enter at one end and leave at the other end. Rather current paths are as shown in Fig. 5.22. This might

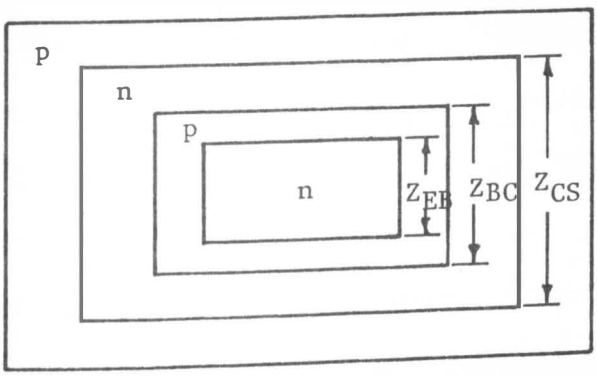



Fig. 5.21 Top view of a fabricated n-p-n transistor.

complicate and cause extra factors to be taken into account for a more

accurate analysis. But since we are concerned with explaining an observed trend we will assume a rather simple model of diode as if contacts are made at two opposite ends.

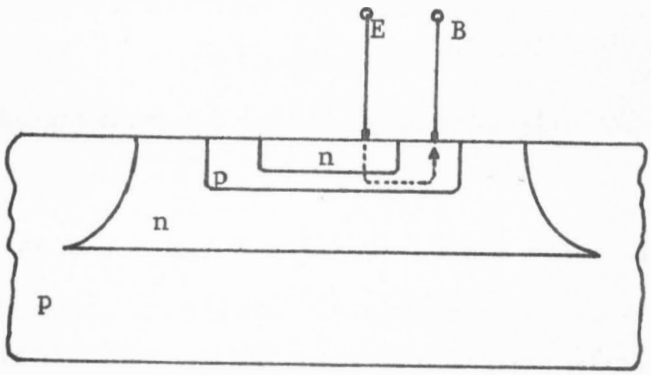



Fig. 5.22 Current path in E-B junction of an n-p-n transistor.

To explain the shift between p-n junction characteristics, we start with a simple diode model. When a negative potential is applied to the n-region relative to the p-region in a simple p-n junction, excess electrons will be pushed into the n-region and excess holes into the p-region. Thus the electron and hole concentration will both be above their respective equilibrium values and therefore the pn product will exceed $n_i^2$, throughout portions of the semiconductor. Under such injection conditions the carrier concentrations will attempt to return to their equilibrium value by recombination. In the steady state, electrons and holes disappearing through recombination will be replenished by more electrons and holes coming in through the contacts to the n and p regions respectively. This gives rise to a forward current.

Three regions can be distinguished as illustrated in Fig. 5.23:

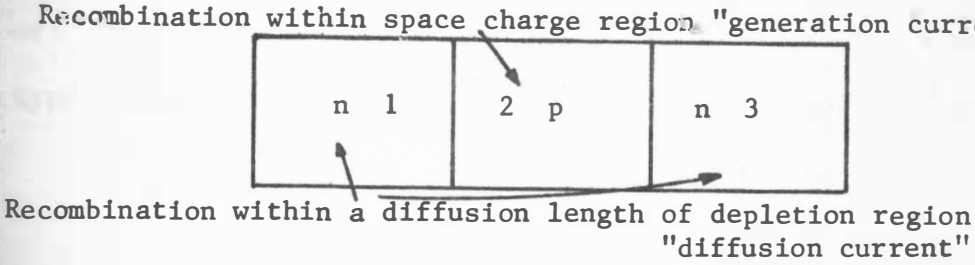



Fig. 5.23 Illustration of mechanism giving rise to forward current.

the neutral regions 1 and 3 adjacent to the space charge region and space charge region-2 itself. Thus, flux of electrons entering through the contact is given by:

$I_F/q$ = (number of electrons recombining with holes in neutral n-region (1) per unit area)

+ (number of electrons recombining with holes in space charge region (2) per unit area)

+ (number of electrons recombining with holes in neutral p-region (3) per unit area)

Current components-1 and 3 are called diffusion currents and current component-2 is called the recombination current.

According to Grove[4] for a step junction--

$$I_{diffusion} = -qD \frac{n_i^2 A_J}{C_B \cdot L} \exp\left[\frac{q|V_F|}{KT}\right] \tag{5.7}$$

$$I_{recombination} = -\tfrac{1}{2} D \frac{n_i}{\tau} W A_J \exp\left[\frac{q|V_F|}{KT}\right] \tag{5.8}$$

where $n_i$ is intrinsic carrier concentration, D is diffusion coefficient, $\tau$ is lifetime, W is depletion region width, $C_B$ is bulk impurity concen-

tration, $A_J$ is cross sectional area of p-n junction and L is the channel length. We can treat q, D and $n_i$ as constants for a particular type of p-n junction. Then for a fixed forward voltage $V_F$ --

$$I_{diffusion} \propto \frac{A_J}{L \cdot C_B} e^{q|V_F|/KT} \propto \frac{A_J}{L \cdot C_B} \tag{5.9}$$

$$I_{recombination} \propto WA_J e^{q|V_F|/KT} \propto A_J \cdot W \tag{5.10}$$

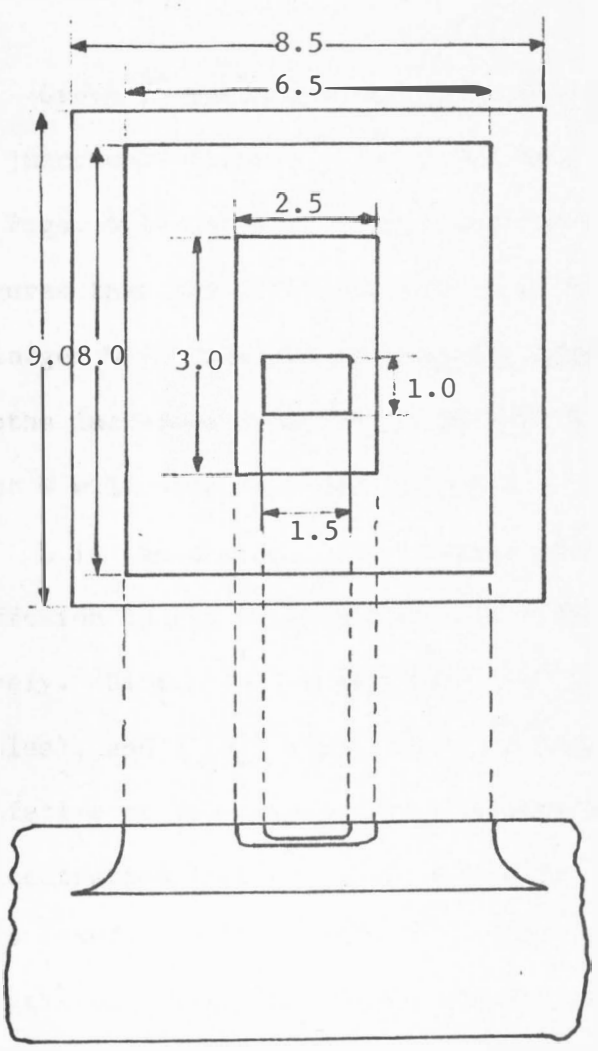
The above expressions relate $I_{diffusion}$ and $I_{recombination}$ to the junction area $A_J$, depletion region width W, channel length L and bulk concentration $C_B$. Variation in all these four quantities -- $A_J$, W, L and $C_B$ for three junctions -- E-B, B-C and C-S must be known to find out the respective diffusion and recombination current variation for these three junctions.

Fig. 5.24 shows the geometry of a monolithic integrated circuit n-p-n transistor.

Table 5.4 lists the approximate X, Y and Z dimensions (Fig. 5.24) and area $A_J$ for all three -- E-B, B-C and C-S junctions.

| Dimension \ Junction | E-B | B-C | C-S |
|---|---|---|---|
| X | 1.5 mil | 2.5 mil | 6.5 mil |
| Y | 2.7 μ | 23 μ | >>23μ |
| Z | 1.0 mil | 3 mil | 8 mil |
| $A_J$ | 1.5 $mil^2$ | 7.5 $mil^2$ | 52 $mil^2$ |

Table 5.4 Approximate dimensions of E-B, B-C and C-S junctions.




Emitter Area
1x1.5 mil$^2$

Base Area
2.5x3 mil$^2$

Substrate Area
6.5x8 mil$^2$

Junction Depths
E-B 2.0μ
B-C 2.7μ
C-S 25μ

Fig. 5.24 Geometry of an n-p-n monolithic transistor.

Still we have to find out how L and W used in Eqns. (5.9) and (5.10) vary for these three junctions. Eqns. (5.7) and (5.8) are true for a step junction. Though in our case junctions are diffused rather than being step, to simplify the analysis we will treat our junctions as step junctions.

Grove[4] has shown the depletion region width W for three types of junctions--diffused, one sided step and linearly graded junction in Figs. 6.14 and 6.15 (pages 168-169). It could be seen from those figures that the depletion region width W increases with junction depth. A larger W is expected if junction depth is larger. Since junction depths increases from E-B to B-C and B-C to C-S junctions, we expect that W will also increase from E-B to B-C and B-C to C-S junctions.

L is the channel length which is a combination of $L_n$ and $L_p$, the diffusion length of electrons and diffusion length of holes respectively. Diffusion lengths depend on $D_n(D_p)$, diffusivity of electron (holes), and $\tau_n(\tau_p)$ lifetime of electrons in p-type semiconductor (lifetime of holes in n-type semiconductor). For a certain impurity concentration in a semiconductor both $\tau_p(\tau_n)$ and $D_p(D_n)$ are more or less fixed. Hence not much variation in $L_n$ or $L_p$, is expected. Since lengths of p-type and n-type regions are very small compared to the typical diffusion lengths, $L_n$ or $L_p$ channel length L is the length of the region itself. The following calculations show the order of magnitude of $L_n$ and $L_p$.

$$L_p = \sqrt{D_p \tau_p} \qquad \text{and} \qquad L_n = \sqrt{D_n \tau_n}$$

$$D_p \simeq 10 \text{ cm}^2/\text{sec} \qquad D_n \simeq 30 \text{ cm}^2/\text{sec}$$

$$\tau_p \simeq 10^{-6} \text{ sec} \qquad \tau_n \simeq 10^{-6} \text{ sec}$$

So

$$L_p \simeq 3\times10^{-3} \text{ cm} \qquad L_n \simeq 5\times10^{-3} \text{ cm}$$

Hence, we can see that $L_p \simeq 3\times10^{-3}\text{cm} >> 2\mu$ length and $L_n \simeq 5\times10^{-3}\text{cm} >> 2\mu$ length.

After determining the nature of variation of L, W and $A_J$ for these three p-n junctions we proceed to determine the nature of varia-

tions of $C_B$ for these junctions. Fig. 5.25 shows the impurity profiles for an IC transistor. Impurity concentration in any region is not constant and decreases with depth of diffusion. Table 5.5 lists impurity concentrations available near the top of each region along with $A_J$ and L. Here $L_n$ and $L_p$ are just the depth of diffusion because as said before $\sqrt{D_p \tau_p}$ is several orders of magnitude larger than the junction depths.

| Junction | $A_J(mil^2)$ | $(C_B)_n$ | $(C_B)_p$ | $L_p$ | $L_n$ |
|---|---|---|---|---|---|
| E-B | 1.5 | $10^{21}/cm^3$ | $\sim 2\times10^{17}/cm^3$ | $2\mu$ | $0.7\mu$ |
| B-C | 7.5 | $\sim 2\times10^{17}/cm^3$ | $1.2\ 10^{16}/cm^3$ | $\sim 22\mu$ | $0.7\mu$ |
| C-S | 52 | $1.2\times10^{16}/cm^3$ | $1.4\times10^{15}/cm^3$ | $\sim 22\mu$ | $>>22\mu$ |

Table 5.5 Junction area, diffusion length and bulk impurity concentration of three p-n junctions in the transistor.

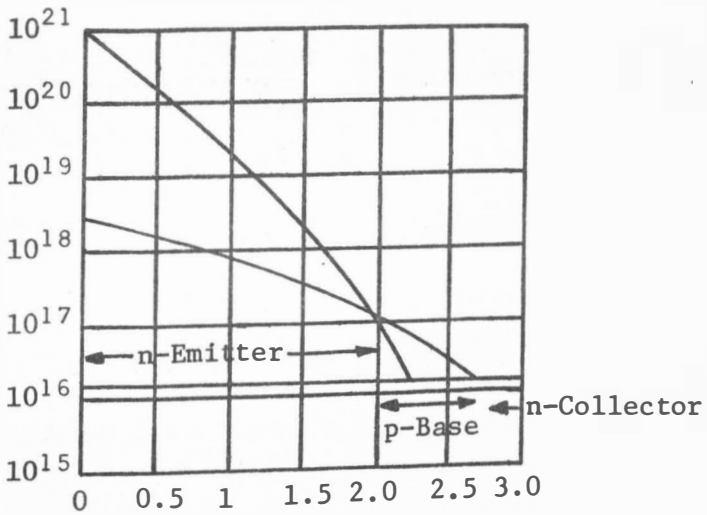



Fig. 5.25 Impurity profiles for an IC transistor.

Table 5.6 lists the impurity bulk concentrations considered near the middle of each region for three junctions.

| Junction | $(C_B)_n$ /cm$^3$ | $(C_B)_p$ /cm$^3$ |
|---|---|---|
| E-B | $2\times10^{20}$ | $\sim7\times10^{16}$ |
| B-C | $\sim7\times10^{16}$ | $\sim1.2\times10^{16}$ |
| C-S | $1.2\times10^{16}$ | $1.4\times10^{15}$ |

Table 5.6 Bulk impurity concentration for three p-n junctions in the transistor.

Table 5.7 shows the variation of total diffusion current ($I_{diff}$) calculated for two cases of impurity concentrations for all three junctions in a transistor.

| Junction | $I_{diff}$ when $C_B$ considered near top of the region | $I_{diff}$ when $C_B$ considered near the middle of the region |
|---|---|---|
| E-B | $\propto 3.7\times10^{-18}$ | $\propto 1\times10^{-17}$ |
| B-C | $\propto 8\times10^{-17}$ | $\propto 1.5\times10^{-16}$ |
| C-S | $\propto 1.7\times10^{-15}$ | $\propto 1.7\times10^{-15}$ |

Table 5.7 Variation of diffusion current for three p-n junctions in the transistor.

From this table we find that diffusion current, in any case, will increase from E-B to B-C to C-S junction. From previous discussion, W and $A_J$ both increase from E-B to B-C to C-S junctions. Since recombination current varies directly with both $A_J$ and W (Eqn. (5.10)), recombination current will also increase from E-B to B-C to C-S junctions. For very low values of forward current recombination current dominates

and since recombination current increases from E-B to B-C to C-S junctions total forward current also increases in the same fashion. When diffusion current starts dominating in forward current, because diffusion current increases rapidly than the recombination current from E-B to B-C to C-S junctions ($C_B$ varies more rapidly than $A_J$), forward current will also increase for these junctions in that order. This suggests that forward current $I_F$ will be less for E-B junction than for B-C junction for a particular forward voltage $V_F$. Similarly $I_F$ for B-C junction will be less than for C-S junction. This leads to progressively higher points for E-B to B-C to C-S junctions on the ordinate for a fixed point on the abscissa in the V-I plane. Fig. 5.26 shows the relative position of V-I curves for these three junctions.

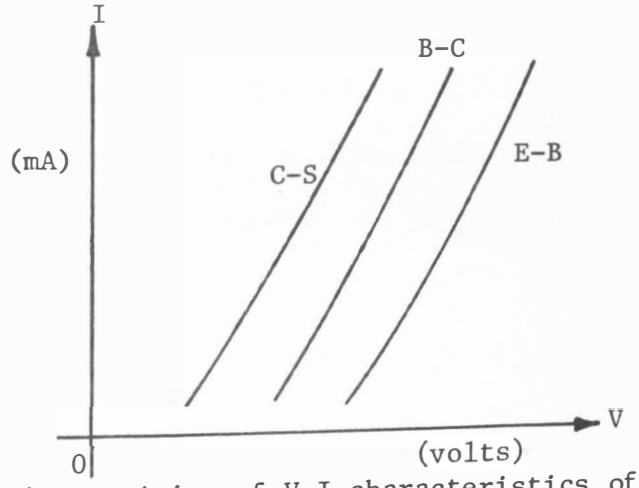



Fig. 5.26 Relative position of V-I characteristics of E-B, B-C and C-S junctions.

After explaining the shift observed in V-I characteristic for the three junctions we will now look into the nature of variation of I with V for these junctions.

As said earlier forward current $I_F$ is a combination of diffusion and recombination currents. We can distinguish the recombination current component from the diffusion current component by their different voltage dependences which correspond to a slope of q/2KT and q/KT, respectively, in a semi-log representation. We can observe the change in slope as the diffusion current begins to dominate with increasing forward bias for a silicon diode. A simple empirical representation of the forward current-voltage characteristics is given by the formula

$$I_F \propto \exp\left[q|V_F|/mKT\right] \tag{5.11}$$

where the empirical factor is m=1 for pure diffusion current and m=2 for pure recombination current, provided the simple theory is applicable. When both currents are comparable, m will vary between 1 and 2.

It was decided to find out how closely the theoretical Eqn. (5.11) fits the observed V-I characteristics. Arbitrarily, one junction (E-B) of transistor $Q_3$ was selected to compare the characteristics. Fig. 5.27 shows the V-I characteristics of E-B junction of $Q_3$ compared to theoretical plots for the two cases of m=1.2 and m=1.53 (Eqn. (5.11)). The constant of proportionality was adjusted to start the calculated curves near the measured one. It can be seen that curve for m=1.2 is very close to the experimentally observed curve over three order of magnitude. Deviation occurs for currents above 0.1 mA. Perhaps other effects, which were not taken into account, like surface effects, depletion region recombination effects, high injection and emitter crowding effects, etc. take over to make it necessary to modify Eqn.

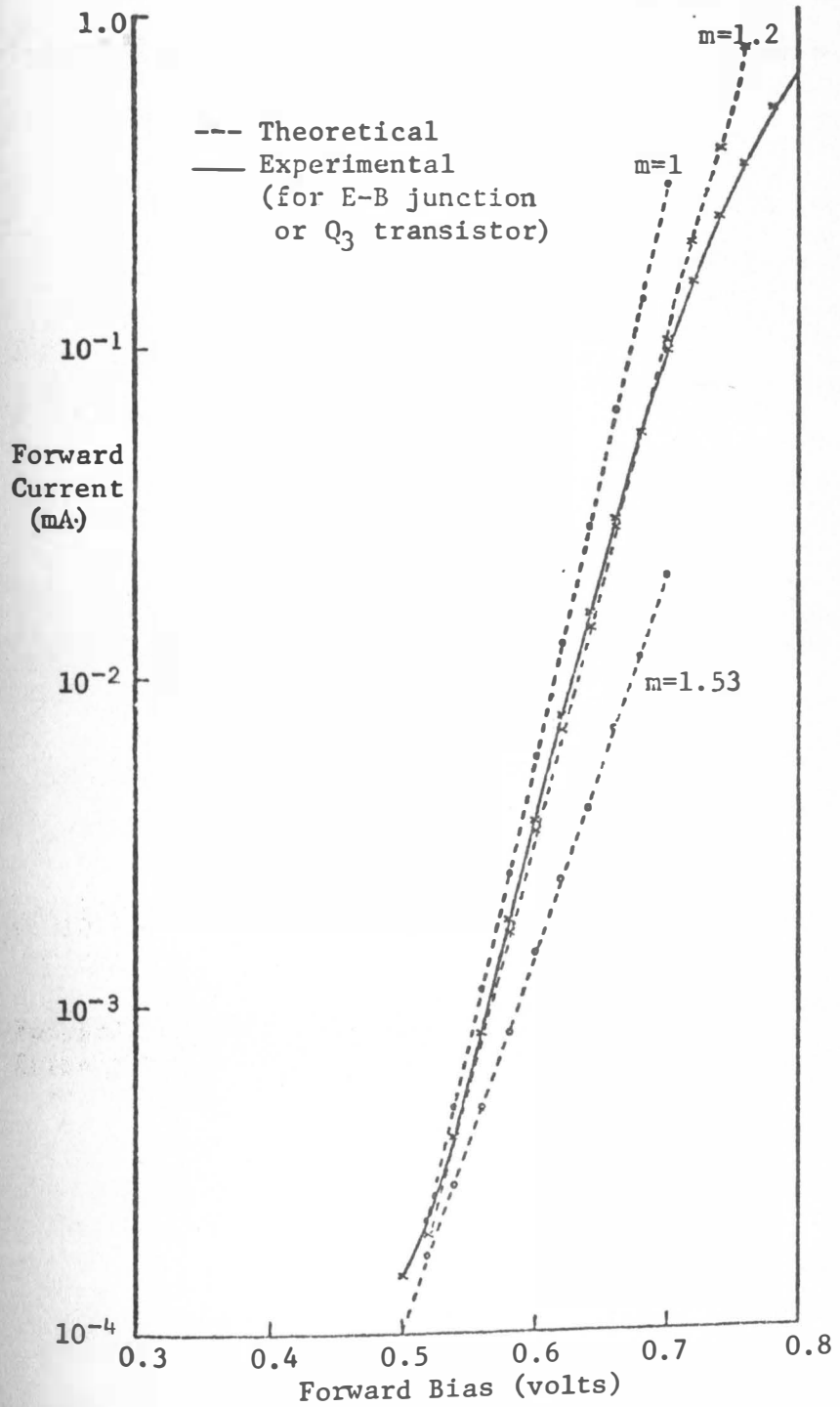



Fig. 5.27 Comparison of experimental and theoretical V-I variation for a forward biased diode.

(5.11). These effects are not explored in this thesis. Thus we see that observed nature of V-I characteristics for p-n junctions satisfy the theoretical expression over a range.

# CHAPTER VI

## CONCLUSIONS

This research was instituted to study monolithic circuit elements, with emphasis on the parasitic effects associated with them. Quick chip SG 3801 was selected because it contains a number of monolithic elements. This is a monolithic breadboard and the elements can be interconnected with nothing more than a wire bonding machine. Quick chip SG 3801 contains high frequency n-p-n, medium current n-p-n, lateral p-n-p and common collector p-n-p transistors, base-emitter junction diodes, zener diodes, center tapped resistors with values ranging from 30Ω to 20KΩ, pinch resistors with values above 25KΩ and junction capacitors.

Monolithic resistors are formed by diffusion into a background region of the opposite conductivity type. Resistors are usually made during the base diffusion. The junction formed between the resistor and the epitaxial layer (collector) gives rise to parasitic capacitance. This affects the frequency response of the resistors. At the high frequency end of the spectrum, the parasitic effect of the junction capacitance severely affects the behavior of a monolithic resistor. In this study a model was developed which can predict the frequency behavior of the resistor. Magnitude and phase of the impedance looking in at the input terminals, and the equivalent parallel resistance $R_p$ and

capacitance $C_p$ were observed against frequency.

There are three different configurations in which a resistor can be used:

(a) Resistor with one end connected to substrate (configuration-A)

(b) Two ends of resistor with substrate floating (configuration-B)

(c) As a transfer block (configuration-C).

Fig. 2.6 shows all these configurations. It would be ideal if a model could be obtained which would predict the frequency response for all these configurations. It was determined that two models are required. One model predicts the frequency response for configurations-A and C and other one for configuration-B. Since the nature of parasitic capacitance is distributed, a distributed network model was chosen. It was found that there is about an optimum number of segments in a distributed RC network which gives rise to good agreement between calculated and measured values. A ten segment RC network was determined to be valid. In these networks two variations are possible:

(a) Initial series resistance network(Fig. 4.8(a))

(b) Initial shunt capacitance network(Fig. 4.8(b))

From these, the initial shunt capacitance model was selected because it provides larger phase responses that fit more closely to the actual observed responses.

In a diffused resistor, the substrate always provides some small amount of series resistance. It was found that taking this substrate resistance into account, for low values of diffused resistors, the predicted frequency response is improved. Substrate resistance of

1-10% of the total dc resistance in each section provided a good model.

Fig. 4.42 shows the final models for three values of resistors with chip values of 600Ω, 2.5KΩ and 10KΩ (±20% tolerance). Actual values were 760Ω, 2.85Ω and 11.1KΩ respectively. The figure shows models for all three configurations and the actual values of $R_s$ and $C_s$ used. $R_s$ is the sectional resistance, $C_s$ is the sectional capacitance and NR gives the substrate resistance in each section, while R is the low frequency value of the resistance measured for the resistor.

Values of sectional capacitances and resistances could be found as follows. For configurations-A and C, the value of the sectional resistance is one-tenth of the low frequency value of resistor. For the sectional capacitance value, measurement of equivalent parallel capacitance is required. For a ten segment initial shunt capacitance distributed network, eleven capacitive segments are required. Thus $C_s$ is one-eleventh of the total equivalent parallel capacitance $C_p$ measured at a low reference frequency (0.5 MHz) for each configurations-A and C respectively with output port left open. In equation form:

$$R_s = \frac{\text{Value of diffused resistor at low frequency (0.5 MHz)}}{10}$$

$$C_s = \frac{\text{Equivalent parallel capacitance with output port open}}{11}$$

For configuration-B, the value of $R_s$ is obtained in the same way as for the other configurations. Value of sectional capacitance $C_s$ can be obtained by measuring equivalent parallel capacitance $C_p$, at low frequency (0.5 MHz) for the resistor connected in configuration-B.

Diodes were studied, and diode capacitance was first taken into consideration. Here again it was desired to have a simple model that would agree with observed behavior. Diodes on the chip are emitter-base junction diodes. Four connections--A, B, C and D (Figs. 5.6, 5.7, 5.8 and 5.9) were used in the study. It was observed that the equivalent parallel resistance of a reverse biased diode decreases with increasing frequency, starting with a nearly infinite value and decreasing to as low as 600Ω at 200 MHz while the equivalent parallel capacitance stays almost constant with increasing frequency. This might lead one to conclude that diode performance deteriorates as frequency increases, but analysis of the simple diode model (Fig. 5.10) shows that it is indeed a simple phenomenon. With increasing frequency the magnitude of impedance of junction capacitance shunting the leakage resistance of a reverse biased junction decreases. This effectively reduces the impedance looking in at input terminals. At low frequencies, the reactance of junction capacitance is large. Since the magnitude of base spreading resistance $r_{bb'}$ is small, for low frequencies the equivalent circuit of diode can be approximated by junction capacitance and leakage resistance only. So looking in at input terminals, equivalent parallel resistance $R_p$ will be the leakage resistance R and equivalent parallel capacitance $C_p$ will be the junction capacitance C. At high frequencies (in our case near 200 MHz) reactance of junction capacitance is small (nearly 160Ω for a typical 5 pF junction capacitance). So equivalent circuit can be approximated by base spreading resistance $r_{bb'}$ in series with junction capacitance C. It can be seen that look-

ing in at input terminals, this will give a small value of equivalent parallel resistance (∿600Ω) and a equivalent parallel capacitance nearly of same value as junction capacitance. At extremely high frequencies, in limit, $R_p$ will approach $r_{bb'}$ when C shunts all R and $C_p$ will be much lower than C. A more rigorous analysis is presented in Section 5.3.

From the nature of variation of capacitances for different connections-A through D it was found that no simple model could explain all the capacitance variation trends. A model (e.g. Fig. 5.13) could explain the capacitance values of three different connections but not all four. No simple model could be developed to explain the capacitance variation trend for different connections. Since no simple model could be found for diodes, it was considered worthwhile to compare the actual diodes on the chip to the E-B junction diodes obtained from using transistors on the chip. A medium current n-p-n transistor was used in two connections: (a) collector shorted to base; and (b) collector left floating, $I_c$=0. On comparison it was found that the trend of capacitance variation for the collector shorted to base case was closer to the actual capacitance variation trend of the diodes. This provides us with a contradiction because the diodes are E-B junction diodes and nothing seems to suggest that they have collector-to-base short circuits. Thus there seems to be some extraneous factor which is modifying the capacitance variation trend for these connections and providing values different from those expected from use of a simple model.

D-C input characteristics of various transistor junctions were studied. As noted earlier, there are four types of transistors available

on the chip--high frequency n-p-n, medium current n-p-n, lateral p-n-p and common collector p-n-p. The method of fabrication and the geometry of these transistors differ. V-I characteristics were obtained for all the junctions (E-B, B-C and C-S, B-S in case of lateral p-n-p) and compared.

It was found that a shift is observed for E-B junctions from B-C junction and for B-C from C-S junction. V-I curves for C-S junctions are on the extreme left while E-B junction characteristic curves are on extreme right with B-C curve falling in between. This trend is observed for all transistor types. The forward current has two current components--$I_{diffusion}$ and $I_{recombination}$. For constant D, $n_i$ and $\tau$ --

$$I_{diffusion} \propto \frac{A_J}{L \cdot C_B}$$

and

$$I_{recombination} \propto WA_J$$

where $A_J$ is junction area and L is channel length and $C_B$ is bulk impurity concentration. For typical diffused monolithic transistors it was found that $A_J$ increases from E-B to B-C to C-S junctions in that order. Not much variation in W is expected because we are considering the characteristics under the same set of conditions. Since all the three diodes are narrow base diodes (i.e. length of doped region< $\sqrt{D\tau}$ ) channel length L also changes according to the diffusion depth of these junctions. Impurity concentration $C_B$ varies significantly from one junction to another according to Fig. 5.25. Due to the predominant effect of $C_B$ over L total diffusion current decreases gradually

from C-S to B-C and from B-C to E-B junctions. Since area $A_J$ also changes in that order it tries to help total diffusion current vary in the same fashion. Due to the increase of both $A_J$ and W from E-B to B-C to C-S junctions, recombination current also increases for these junctions in that order. For very small forward bias recombination current dominates and because it increases from E-B to B-C to C-S junctions forward current also increases. When diffusion current takes over then forward current still increases because diffusion current increases from E-B to B-C to C-S junctions. It is important to note that diffusion current increases more rapidly than recombination current with increasing forward bias voltage. Thus it can be expected that for C-S junction the forward current $I_F$ will be larger than for B-C and for B-C it would be larger than E-B junction for same value of forward voltage. This plots higher points on ordinate for C-S junction than for B-C and for B-C than for E-B junction in V-I plane. Thus the shift of the V-I characteristics is due to the junction area and impurity concentration of various junctions.

Regarding the nature of variation of I vs. V for any individual junction, it was found that forward current follows a simple law:

$$I_F \propto e^{qV_F/mKT}$$

with empirical factor m varying from m=1 for pure diffusion current to m=2 for pure recombination current. In our case m=1.2 fits well to one of the V-I characteristics of E-B junction of n-p-n transistor for three orders of magnitude. After that some deviation is observed and

no longer a simple model is valid. Factor m might vary from one transistor to another and from one junction to another.

# BIBLIOGRAPHY

## References Cited in the Thesis

1. Dicken, H., "Designing Diffused Integrated Circuit Resistor," Electronic Industries, Vol. 21, No. 10, pp. 88-91, October 1962.

2. Fogiel, M., Microelectronics, Research and Education Association, New York, N.Y., 1968.

3. Ghandhi, S. K., The Theory and Practice of Microelectronics, John Wiley and Sons, Inc., New York, 1968.

4. Grove, A. S., Physics and Technology of Semiconductors Devices, John Wiley and Sons, Inc., New York, 1967.

5. Lynn, D. K., Meyer, C. S., and Hamilton, D. J., Analysis and Design of Integrated Circuits, McGraw-Hill Book Co., New York, 1967.

6. Staff of Science and Technology Aerospace Division, Westinghouse Electric Corporation, Integrated Electronic Systems, Prentice-Hall, Inc., Englewood Cliffs, New Jersey, 1970.

## Other References

7. Camenzind, H. R., Circuit Design for Integrated Electronics, Addison-Wesley Publishing Co., Reading, Mass., 1968.

8. Donovan, R. P., et al., Integrated Silicon Device Technology, Vol. I--Resistance, Technical Documentary Report No. ASD-TDR-63-316, Research Triangle Institute, Durham, N. Carolina, 1963.

9. Lin, H. C., Integrated Electronics, Holden-Day, Inc., San Francisco, 1967.

10. Warner, R. M., Jr., and Fordemwalt, J. N., Integrated Circuits, McGraw-Hill, New York, 1965.

# APPENDIX

This appendix contains the tabulated values of equivalent parallel resistance and capacitance for various connections of diodes on the chip and those connected from the transistors.

| Frequency (MHz) | No Bias | | | | 5 V reverse bias | | | |
|---|---|---|---|---|---|---|---|---|
| | E=pin5 $R_p$(KΩ) | B=pin4 $C_p$(pF) | E=pin4 $R_p$(KΩ) | B=pin5 $C_p$(pF) | E=pin5 $R_p$(KΩ) | B=pin4 $C_p$(pF) | E=pin4 $R_p$(KΩ) | B=pin5 $C_p$(pF) |
| 0.5 | ∞ | 2.05 | ∞ | 1.6 | ∞ | 1.45 | ∞ | 1.4 |
| 1.0 | ∞ | 1.9 | ∞ | 1.7 | ∞ | 1.45 | ∞ | 1.3 |
| 2.0 | ∞ | 1.9 | ∞ | 1.7 | ∞ | 1.46 | ∞ | 1.3 |
| 4.0 | ∞ | 1.9 | ∞ | 1.8 | ∞ | 1.48 | ∞ | 1.3 |
| 8.0 | ∞ | 1.9 | ∞ | 1.8 | ∞ | 1.48 | ∞ | 1.3 |
| 10 | ∞ | 1.87 | ∞ | 1.8 | ∞ | 1.5 | ∞ | 1.4 |
| 20 | >100 | 1.89 | >100 | 1.8 | >100 | 1.49 | ∞ | 1.26 |
| 40 | 70 | 1.89 | 80 | 1.8 | 80 | 1.47 | >100 | 1.3 |
| 60 | 35 | 1.88 | 34 | 1.85 | 50 | 1.48 | 80 | 1.31 |
| 80 | 21 | 1.8 | 19 | 1.92 | 28 | 1.47 | 46 | 1.3 |
| 100 | 11.5 | 1.8 | 11.2 | 1.91 | 16 | 1.49 | 32 | 1.3 |
| 120 | 8 | 1.82 | 8 | 1.9 | 12 | 1.46 | 23 | 1.3 |
| 140 | 5.8 | 1.81 | 5.7 | 1.9 | 9.4 | 1.46 | 16.5 | 1.32 |
| 180 | 3.75 | 1.88 | 3.6 | 1.89 | - | - | 6.4 | 1.3 |
| 200 | 3.6 | 2.05 | 2.55 | 2.25 | 4.2 | 1.48 | 6.1 | 1.31 |

Table I (a) Parasitic measurements for connection-A (for diode-1)

| Frequency (MHz) | No Bias | | | | 5 V Reverse Bias | | | |
|---|---|---|---|---|---|---|---|---|
| | E=pin7 $R_p$(KΩ) | B=pin6 $C_p$(pF) | E=pin6 $R_p$(KΩ) | B=pin7 $C_p$(pF) | E=pin6 $R_p$(KΩ) | B=pin7 $C_p$(pF) | E=pin7 $R_p$(KΩ) | B=pin6 $C_p$(pF) |
| 0.5 | ∞ | 1.9 | ∞ | 1.6 | ∞ | 1.28 | ∞ | 1.48 |
| 1 | ∞ | 1.87 | ∞ | 1.58 | ∞ | 1.25 | ∞ | 1.5 |
| 2 | ∞ | 1.92 | ∞ | 1.61 | ∞ | 1.22 | ∞ | 1.41 |
| 4 | ∞ | 1.92 | ∞ | 1.62 | ∞ | 1.22 | ∞ | 1.45 |
| 8 | ∞ | 1.89 | ∞ | 1.6 | ∞ | 1.25 | ∞ | 1.43 |
| 10 | ∞ | 1.9 | ∞ | 1.65 | ∞ | 1.22 | ∞ | 1.46 |
| 20 | >100 | 1.89 | >100 | 1.65 | ∞ | 1.26 | >100 | 1.46 |
| 40 | 80 | 1.86 | ∿100 | 1.65 | >100 | 1.23 | 100 | 1.46 |
| 60 | 32 | 1.85 | 41 | 1.7 | 80 | 1.26 | 45 | 1.46 |
| 80 | 18.3 | 1.87 | 26 | 1.7 | 50 | 1.22 | 29 | 1.47 |
| 100 | 11.3 | 1.83 | 15 | 1.7 | 30 | 1.26 | 16.5 | 1.47 |
| 120 | 7.6 | 1.82 | 9.65 | 1.7 | 18.5 | 1.29 | 11 | 1.47 |
| 140 | 5.3 | 1.89 | 6.4 | 1.75 | 12.7 | 1.3 | 7.5 | 1.49 |
| 180 | 3.2 | 1.86 | 3.4 | 1.8 | 6.7 | 1.38 | 4.3 | 1.51 |
| 200 | 3.15 | 1.94 | 1.97 | 1.75 | 4.25 | 1.5 | 3.3 | 1.58 |

Table I (b) Parasitic measurements for connection-A (for diode-2).

| Frequency (MHz) | Diode-1 | | | | Diode-2 | | | |
|---|---|---|---|---|---|---|---|---|
| | No Bias | | 5V Reverse Bias | | No Bias | | 5V Reverse Bias | |
| | $R_p$(KΩ) | $C_p$(pF) | $R_p$(KΩ) | $C_p$(pF) | $R_p$(KΩ) | $C_p$(pF) | $R_p$(KΩ) | $C_p$(pF) |
| 0.5 | ∞ | 3.0 | ∞ | 2.51 | ∞ | 2.85 | ∞ | 2.72 |
| 1 | ∞ | 2.92 | ∞ | 2.51 | ∞ | 2.9 | ∞ | 2.66 |
| 2 | ∞ | 2.86 | ∞ | 2.45 | ∞ | 2.91 | ∞ | 2.65 |
| 4 | ∞ | 2.9 | ∞ | 2.5 | ∞ | 2.62 | ∞ | 2.58 |
| 8 | ∞ | 2.8 | ∞ | 2.49 | ∞ | 2.91 | ∞ | 2.53 |
| 10 | >100 | 2.95 | >100 | 2.52 | >100 | 3.0 | >100 | 2.72 |
| 20 | 70 | 2.92 | 80 | 2.58 | 70 | 3.0 | ∿80 | 2.7 |
| 40 | 119.7 | 2.88 | 22 | 2.58 | 21 | 2.92 | ∿22 | 2.68 |
| 60 | 9.5 | 2.65 | 9.8 | 2.58 | 9 | 3.05 | 9.8 | 2.71 |
| 80 | 5 | 2.85 | 5.38 | 2.58 | 5.1 | 2.99 | 5.6 | 2.7 |
| 100 | 3.13 | 2.85 | 3.45 | 2.56 | 3.2 | 2.95 | 3.55 | 2.66 |
| 120 | 2.2 | 2.92 | 2.55 | 2.52 | 2.0 | 3.0 | 2.2 | 2.71 |
| 140 | 1.84 | 2.8 | 1.94 | 2.52 | 1.51 | 2.99 | 1.63 | 2.71 |
| 180 | 0.925 | 2.86 | 1.05 | 2.50 | 0.93 | 2.94 | 0.99 | 2.68 |
| 200 | 0.82 | 2.85 | 0.82 | 2.48 | 0.82 | 3.05 | 0.86 | 2.68 |

Table II. Parasitic measurements for configuration-B.

| Frequency (MHz) | Diode-1 No Bias $R_p$(KΩ) | Diode-1 No Bias $C_p$(pF) | Diode-2 No Bias $R_p$(KΩ) | Diode-2 No Bias $C_p$(pF) |
|---|---|---|---|---|
| 0.5 | ∞ | 1.9 | ∞ | 1.85 |
| 1 | ∞ | 1.95 | ∞ | 1.75 |
| 2 | ∞ | 1.85 | ∞ | 1.72 |
| 4 | ∞ | 1.9 | ∞ | 1.71 |
| 8 | ∞ | 1.85 | ∞ | 1.69 |
| 10 | ∞ | 1.82 | ∞ | 1.7 |
| 20 | >100 | 1.78 | >100 | 1.69 |
| 40 | 75 | 1.75 | 75 | 1.69 |
| 60 | 32 | 1.78 | 32 | 1.68 |
| 80 | 18 | 1.77 | 18 | 1.72 |
| 100 | 11.2 | 1.77 | 11 | 1.68 |
| 120 | 6.4 | 1.83 | 6.7 | 1.73 |
| 140 | 4.85 | 1.85 | 4.55 | 1.8 |
| 180 | 2.87 | 1.89 | 2.25 | 1.86 |
| 200 | 2.25 | 1.81 | ∿2.1 | ∿1.98 |

Table III Parasitic measurements for connection-C.

| Frequency (MHz) | Diode-1 | | | | Diode-2 | | | |
|---|---|---|---|---|---|---|---|---|
| | No Bias | | 5V Reverse Bias | | No Bias | | 5V Reverse Bias | |
| | $R_p$(KΩ) | $C_p$(pF) | $R_p$(KΩ) | $C_p$(pF) | $R_p$(KΩ) | $C_p$(pF) | $R_p$(KΩ) | $C_p$(pF) |
| 0.5 | ∞ | 2.25 | ∞ | 1.75 | ∞ | 1.52 | ∞ | 1.5 |
| 1 | ∞ | 1.7 | ∞ | 1.7 | ∞ | 1.52 | ∞ | 1.5 |
| 2 | ∞ | 1.7 | ∞ | 1.7 | ∞ | 1.5 | ∞ | 1.5 |
| 4 | ∞ | 1.68 | ∞ | 1.6 | ∞ | 1.52 | ∞ | 1.5 |
| 8 | ∞ | 1.89 | ∞ | 1.6 | ∞ | 1.52 | ∞ | 1.51 |
| 10 | ∞ | 1.6 | ∞ | 1.6 | ∞ | 1.52 | ∞ | 1.54 |
| 20 | ∞ | 1.62 | ∞ | 1.6 | >100 | 1.52 | >100 | 1.5 |
| 40 | >100 | 1.61 | >100 | 1.6 | $100^+$ | 1.53 | $100^+$ | 1.51 |
| 60 | 90 | 1.6 | ∿90 | 1.6 | 95 | 1.52 | 100 | 1.51 |
| 80 | 60 | 1.63 | ∿60 | 1.6 | 48 | 1.58 | 60 | 1.51 |
| 100 | 30 | 1.62 | 29 | 1.61 | 35 | 1.55 | 36 | 1.55 |
| 120 | 19.5 | 1.63 | 20 | 1.6 | 20 | 1.55 | 23 | 1.55 |
| 140 | 12.5 | 1.7 | 14 | 1.65 | 15.8 | 1.6 | 16.5 | 1.58 |
| 180 | 6.4 | 1.79 | 6.9 | 1.72 | 10.6 | 1.65 | 10.2 | 1.62 |
| 200 | ∿5 | 1.73 | 5 | 1.72 | - | | - | - |

Table IV Parasitic measurements for connection-D.

| Frequency (MHz) | No Bias E=pin8 B=pin10 $R_p$(KΩ) | $C_p$(pF) | No Bias E=pin10 B=pin8 $R_p$(KΩ) | $C_p$(pF) |
|---|---|---|---|---|
| 1 | ∞ | 1.85 | ∞ | 1.75 |
| 4 | ∞ | 1.85 | ∞ | 1.78 |
| 10 | ∞ | 1.8 | ∞ | 1.72 |
| 20 | ∞ | 1.85 | ∞ | 1.8 |
| 40 | >100 | 1.8 | >100 | 1.79 |
| 80 | 32 | 1.8 | 27 | 1.8 |
| 120 | 12 | 1.82 | 11.2 | 1.85 |

Table V Parasitic measurements for connection-A (E-B junction diode, collector floating).

| Frequency (MHz) | No Bias B=pin8, E=pin10 C=pin1 $R_p$(KΩ) | $C_p$(pF) |
|---|---|---|
| 1 | ∞ | 2.4 |
| 4 | ∞ | 2.39 |
| 10 | ∞ | 2.45 |
| 20 | >100 | 2.3 |
| 40 | 8.0 | 2.33 |
| 80 | 13.1 | 2.45 |
| 120 | 6.1 | 2.4 |

Table VI Parasitic measurements for connection-B (E-B junction diode, collector floating).

| Frequency (MHz) | No Bias E=pin10, B=pin1 $R_p$(KΩ) | $C_p$(pF) | No Bias E=pin1, B=pin10 $R_p$(KΩ) | $C_p$(pF) |
|---|---|---|---|---|
| 1 | ∞ | 2.3 | ∞ | 2.9 |
| 4 | ∞ | 2.28 | ∞ | 2.92 |
| 10 | ∞ | 2.28 | ∞ | 2.9 |
| 20 | >100 | 2.3 | >100 | 2.92 |
| 40 | 80 | 2.26 | 50 | 2.9 |

Table VII Parasitic measurements for connection-C (E-B junction diode, collector floating).

| Frequency (MHz) | No Bias E=pin8, B=pin10, C=pin1 $R_p$(KΩ) | $C_p$(pF) |
|---|---|---|
| 1 | ∞ | 2.38 |
| 4 | ∞ | 2.32 |
| 10 | ∞ | 2.3 |
| 40 | ∞ | 2.33 |
| 80 | >100 | 2.32 |

Table VIII Parasitic measurements for connection-D (E-B junction diode, collector floating).

| Frequency (MHz) | No Bias E=pin8 B=pin10 $R_p$ (KΩ) | $C_p$ (pF) | No Bias E=pin10 B=pin8 $R_p$ (KΩ) | $C_p$ (pF) |
|---|---|---|---|---|
| 1 | ∞ | 1.95 | ∞ | 2.2 |
| 4 | ∞ | 1.95 | ∞ | 2.2 |
| 10 | ∞ | 1.9 | ∞ | 2.2 |
| 30 | >100 | 1.93 | >100 | 2.2 |
| 60 | 50 | 1.92 | 38 | 2.2 |
| 100 | 19.2 | 1.98 | 14 | 2.25 |
| 140 | 8 | 2.02 | 6.4 | 2.25 |

Table IX Parasitic measurements for connection-A (E-B junction diode, collector shorted to base).

| Frequency (MHz) | No Bias E=pin10, B=pin8, C=pin1 $R_p$ (KΩ) | $C_p$ (pF) |
|---|---|---|
| 1 | ∞ | 4.5 |
| 4 | ∞ | 4.43 |
| 10 | >100 | 4.51 |
| 30 | 25 | 4.55 |
| 60 | 5.38 | 4.6 |
| 100 | 2.05 | 4.58 |
| 140 | 1.0 | 4.55 |

Table X Parasitic measurements for connection-B (E-B junction diode, collector shorted to base).

| Frequency (MHz) | No Bias E=pin10 $R_p$(KΩ) | B=pin1 $C_p$(pF) | No Bias E=pin1 $R_p$(KΩ) | B=pin10 $C_p$(pF) |
|---|---|---|---|---|
| 1 | | 2.75 | ∞ | 2.1 |
| 4 | | 2.72 | ∞ | 2.08 |
| 10 | >100 | 2.73 | ∞ | 2.1 |
| 30 | 90 | 2.85 | >100 | 2.09 |
| 60 | 21 | 2.73 | 30 | 2.09 |
| 100 | 6.2 | 2.9 | 9.8 | 2.11 |
| 150 | 2.4 | 3.0 | 3.5 | 2.2 |

Table XI Parasitic measurements for connection-C (E-B junction diode, collector shorted to base).

| Frequency (MHz) | No Bias E=pin8, B=pin10, C=pin1 $R_p$(KΩ) | $C_p$(pF) |
|---|---|---|
| 1 | ∞ | 2.2 |
| 4 | ∞ | 2.3 |
| 10 | ∞ | 2.3 |
| 30 | ∞ | 2.3 |
| 60 | >100 | 2.33 |

Table XII Parasitic measurements for connection-D (E-B junction diode, collector shorted to base).